TX91

TX Family Computer On Module

- Processor 1.4 GHz ARM® Cortex®-A55 based NXP i.MX 91
- RAM 512 MB LPDDR4 SDRAM (inline ECC)
- ROM 4 GB eMMC
- Power supply 3.3V to 5V
- Size 26 mm SO-DIMM
- Grade Industrial
- Temperature -25°C to 85°C

1.4 GHz Cortex®-A55

Key Features

- ARM® Cortex®-A55, 1.4 GHz
- NXP's EdgeLock® secure enclave
- 24-bit RGB Display support

Connectivity

- Ethernet
  - 10/100 Ethernet with PHY
- 2x USB 2.0
- 8x UART, 7x I²C, 8x SPI, 2x CAN-FD, 1x eMMC/SD
- 3.3V I/O

OS Support

- Linux

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i.MX 91

The i.MX 91 family delivers an optimized blend of security, features, and energy-efficient performance required for the next generation of Linux-based IoT and industrial applications. The i.MX 91 family enables developers to quickly create new Linux-based edge devices. As the entry point into the i.MX 9 series, the i.MX 91 family provides the extensibility and ease of programming that developers need for applications to evolve over time. Hardware and software commonality with the NXP i.MX 93 family provides additional platform options for scaling product lines that maximize re-use of development investments and decreases time to market.

HIGH-PERFORMANCE COMPUTE

The i.MX 91 applications processors feature an Arm® Cortex®-A55 running at up to 1.4 GHz, 256 KB of L2 cache, and support for the Armv8.2 instruction set including virtualized host extensions, and two-level branch prediction, for optimal performance, security, and efficiency when running Linux and RTOS operating systems.

MACHINE LEARNING SUPPORT

The Arm Cortex-A55 processor core includes dual 64-bit Arm NEON floating-point units and supports the Armv8.2 instruction set with Arm DynamIQ technology, with dot product, half-precision float, cache stashing, and atomic operations for CPU-based machine learning applications.

TX Computer on Module

- NXP i.MX 91
- 512MB LPDDR4 SDRAM
- 4GB eMMC
- DIMM200-module (67,6mm x 26 mm x 4mm)

Standard TXCOM pinout:

Highly scalable design options allow a single platform to cover multiple products. Pin-compatible TX modules allow a single PCB as a platform for different features as product needs dictate.

- 4-wire UARTs (x3)
- I2C / PWM
- Serial Audio Interface
- 4-wire SD-Card/SDIO

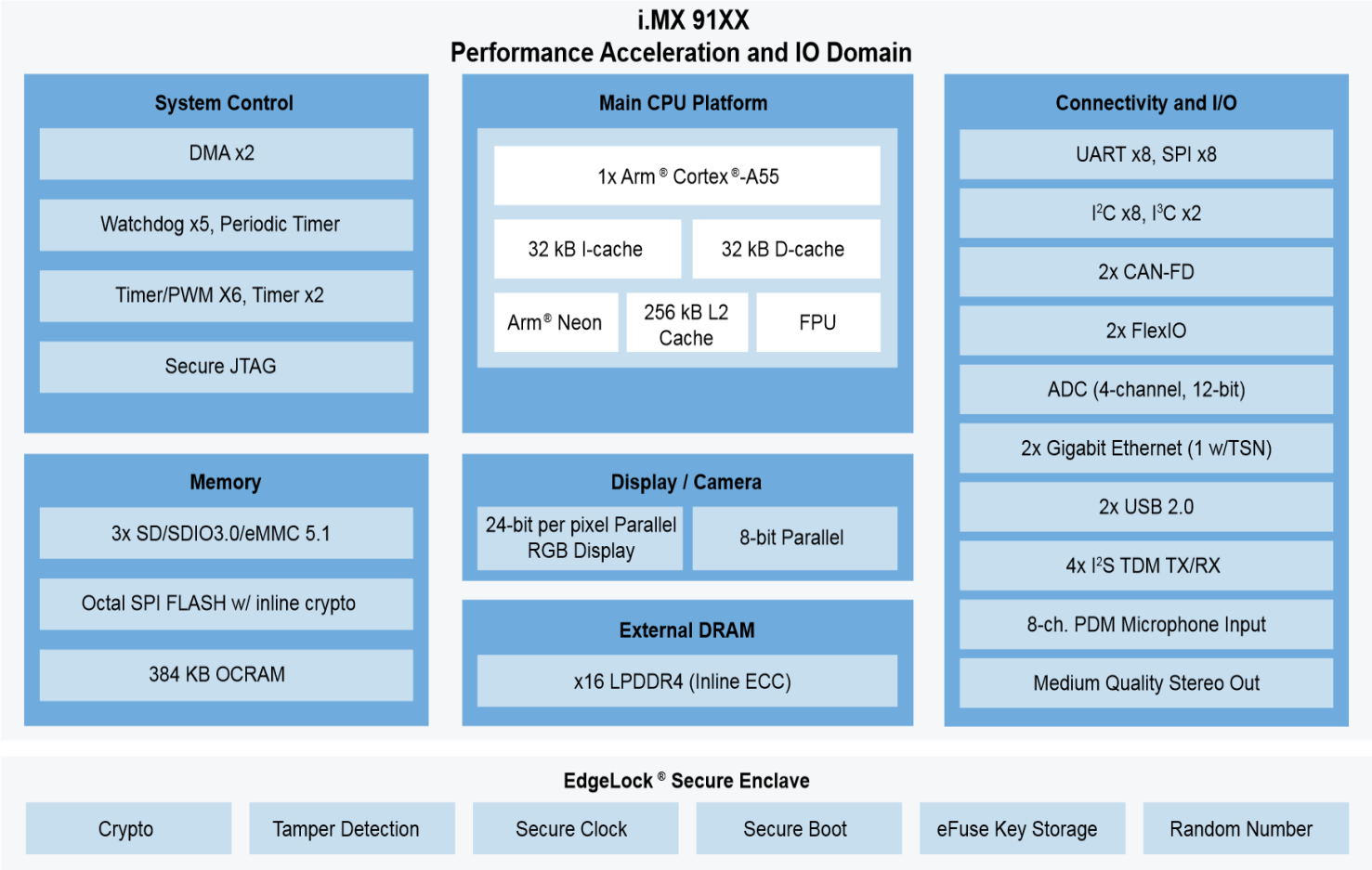
High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- USB 2.0 OTG (Host or Device)

Read more in our TX-Guide:

www.karo-electronics.com/tx-guide

i.MX 91 BLOCK DIAGRAM



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PINOUT

PIN	Type	TX Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
POWER SUPPLY & RESET						
1-4	power	VIN				Module power supply input.
5-7, 9-12	power	VOUT				3.3V power supply output. Supplied by Buck 4
8	3V3	BOOTMODE				Boot mode select H: Boot from eMMC / L: Boot from UART/USB
13	Not connected					
14	3V3			Connected to PMIC IRQ_B		
15	3V3	#RESET_OUT	SD2_RESET_B	USDHC2_RESET_B, LPTMR2_ALT2 FLEXIO1_FLEXIO07, GPIO3_IO07 CCMSRCGPCMIX_SYSTEM_RESET	GPIO3[07]	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controlled by a GPIO function during runtime.
16	5V	#POR		Connected to PMIC_RST_B	10K-PU	PMIC reset input pin.
17	5V	#RESET_IN	POR_B	Connected to PMIC POR_B	10K-PU	
18	GND	GND				
Ethernet						
19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LED2				Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_LED1				Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB-HOST						
27	3V3	USBH_VBUSEN	SD3_DATA0	USDHC3_DATA0 FLEXSPI1_A_DATA00 FLEXIO1_FLEXIO22	GPIO3[22] 10K-PU	Active high VBUS supply enable. This pin can be used to enable a VBUS power supply switch.
28	3V3	#USBH_OC	SD3_DATA1	USDHC3_DATA1 FLEXSPI1_A_DATA01 FLEXIO1_FLEXIO23	GPIO3[23] 10K-PU	Active low over-current indicator input
29	analog	USBH_DM	USB2_D_N			D- pin of the USB cable
30	5V	USBH_VBUS	USB2_VBUS			USB supply voltage input
31	analog	USBH_DP	USB2_D_P			D+ pin of the USB cable
32	GND	GND				
USB-OTG						
33	3V3	USBOTG_ID	USB1_ID			USB PHY ID Detect, no muxing
34	3V3	USBOTG_VBUSEN	SD3_CLK	USDHC3_CLK FLEXSPI1_A_SCLK FLEXIO1_FLEXIO20	GPIO3[20] 10K-PU	Active high VBUS supply enable. This pin can be used to enable a VBUS power supply switch.
35	analog	USBOTG_DM	USB1_D_N			D- pin of the USB cable
36	3V3	#USBOTG_OC	SD3_CMD	USDHC3_CMD FLEXSPI1_A_SS0_B FLEXIO1_FLEXIO21	GPIO3[21] 10K-PU	Active low over-current indicator input connected to a GPIO.
37	analog	USBOTG_DP	USB1_D_P			D+ pin of the USB cable
38	5V	USBOTG_VBUS	USB1_VBUS			USB supply voltage input
39	GND	GND				

PIN	Type	TX Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
I2C						
40	3V3	I2C_DATA	GPIO_IO28	**LPI2C3_SDA** FLEXIO1_FLEXIO28	GPIO2[28]	I2C Data
41	3V3	I2C_CLK	GPIO_IO29	**LPI2C3_SCL** FLEXIO1_FLEXIO29	GPIO2[29]	I2C Clock
PWM						
42	3V3	PWM	I2C2_SCL	LPI2C2_SCL, I3C1_PUR LPUART2_DCB_B, I3C1_PUR_B **TPM2_CH2**, SAI1_RX_SYNC	GPIO1[2]	PWM Output
13	Not connected					
CSPI – Configurable Serial Peripheral Interface						
44	3V3	CSPI_SS	SAI1_TXFS	SAI1_TX_SYNC SAI1_TX_DATA01, **LPSPI1_PCS0** LPUART2_DTR_B, MQS1_LEFT	GPIO1[11]	Slave Select (Selectable polarity) signal
45	3V3	CSPI_SS	SD3_DATA3	USDHC3_DATA3 FLEXSPI1_A_DATA03 FLEXIO1_FLEXIO25	GPIO3[25]	Slave Select (Selectable polarity) signal
46	3V3	CSPI_MOSI	SAI1_RXD0	SAI1_RX_DATA00 SAI1_MCLK, **LPSPI1_SOUT** LPUART2_DSR_B, MQS1_RIGHT	GPIO1[14]	Master Out/Slave In signal
47	3V3	CSPI_MISO	SAI1_TXC	SAI1_TX_BCLK LPUART2_CTS_B, **LPSPI1_SIN** LPUART1_DSR_B, CAN1_RX	GPIO1[12]	Master In/Slave Out signal
48	3V3	CSPI_SCLK	SAI1_TXD0	SAI1_TX_DATA00 LPUART2_RTS_B, **LPSPI1_SCK** LPUART1_DTR_B, CAN1_TX	GPIO1[13]	Serial Clock signal
49	Not connected					
50	GND	GND				
1st SD – Secure Digital Interface						
51	3V3	SD1_CD	SD2_CD_B	**USDHC2_CD_B** ENET_QOS_1588_EVENT0_IN I3C2_SCL, FLEXIO1_FLEXIO00	GPIO3[0]	SD Card Detect
52	3V3	SD1_D[0]	SD2_DATA0	**USDHC2_DATA0** ENET1_1588_EVENT0_OUT CAN2_TX, FLEXIO1_FLEXIO03 CCMSRCGPCMIX_OBSERVE2	GPIO3[3]	
53	3V3	SD1_D[1]	SD2_DATA1	**USDHC2_DATA1** ENET1_1588_EVENT1_IN CAN2_RX, FLEXIO1_FLEXIO04 CCMSRCGPCMIX_WAIT	GPIO3[4]	
54	3V3	SD1_D[2]	SD2_DATA2	**USDHC2_DATA2** ENET1_1588_EVENT1_OUT MQS2_RIGHT, FLEXIO1_FLEXIO05 CCMSRCGPCMIX_STOP	GPIO3[5]	
55	3V3	SD1_D[3]	SD2_DATA3	**USDHC2_DATA3** LPTMR2_ALT1, MQS2_LEFT FLEXIO1_FLEXIO06 CCMSRCGPCMIX_EARLY_RESET	GPIO3[6]	
56	3V3	SD1_CMD	SD2_CMD	**USDHC2_CMD** ENET1_1588_EVENT0_IN I3C2_PUR, I3C2_PUR_B FLEXIO1_FLEXIO02 CCMSRCGPCMIX_OBSERVE1	GPIO3[2]	SD Command bidirectional signal
57	3V3	SD1_CLK	SD2_CLK	**USDHC2_CLK** ENET_QOS_1588_EVENT0_OUT I3C2_SDA, FLEXIO1_FLEXIO01 CCMSRCGPCMIX_OBSERVE0	GPIO3[1]	SD Output Clock.
58	GND	GND				
1st UART						
59	3V3	TXD	UART1_TXD	**LPUART1_TX**, S400_UART_TX LPSPI2_PCS0, TPM1_CH1	GPIO1[5]	1st UART Transmit Data output signal
60	3V3	RXD	UART1_RXD	**LPUART1_RX**, S400_UART_RX LPSPI2_SIN, TPM1_CH0	GPIO1[4]	1st UART Receive Data input signal
61	3V3	RTS/CTS IN	UART2_TXD	LPUART2_TX, **LPUART1_RTS_B** LPSPI2_SCK, TPM1_CH3	GPIO1[6]	1st UART Request to Send no TX standard **output** signal
62	3V3	CTS/RTS OUT	UART2_RXD	LPUART2_RX, **LPUART1_CTS_B** LPSPI2_SOUT, TPM1_CH2 SAI1_MCLK	GPIO1[7]	1st UART Clear to Send no TX standard **input** signal

PIN	Type	TX Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
2nd UART						
63	3V3	TXD	ENET2_TD0	ENET1_RGMII_TD0 **LPUART4_TX**, SAI2_RX_DATA03 FLEXIO2_FLEXIO19	GPIO4[19]	2nd UART Transmit Data output signal
64	3V3	RXD	ENET2_RD0	ENET1_RGMII_RD0 **LPUART4_RX**, SAI2_TX_DATA02 FLEXIO2_FLEXIO24	GPIO4[24]	2nd UART Receive Data input signal
65	3V3	RTS/CTS IN	ENET2_TD1	ENET1_RGMII_TD1 **LPUART4_RTS_B**, SAI2_RX_DATA02 FLEXIO2_FLEXIO18	GPIO4[18]	2nd UART Request to Send no TX standard **output** signal
66	3V3	CTS/RTS OUT	ENET2_RD2	ENET1_RGMII_RD2 **LPUART4_CTS_B**, SAI2_MCLK MQS2_RIGHT, FLEXIO2_FLEXIO26	GPIO4[26]	2nd UART Clear to Send no TX standard **input** signal
3rd UART						
67	3V3	TXD	DAP_TDO_TRACESWO	JTAG_MUX_TDO MQS2_RIGHT, CAN2_RX FLEXIO1_FLEXIO31, **LPUART5_TX**	GPIO3[31]	3rd UART Transmit Data output signal
68	3V3	RXD	DAP_TDI	JTAG_MUX_TDI MQS2_LEFT, CAN2_TX FLEXIO2_FLEXIO30 **LPUART5_RX**	GPIO3[28]	3rd UART Receive Data input signal
69	3V3	RTS/CTS IN	DAP_TMS_SWDIO	JTAG_MUX_TMS FLEXIO2_FLEXIO31 **LPUART5_RTS_B**	GPIO3[29]	3rd UART Request to Send no TX standard **output** signal
70	3V3	CTS/RTS OUT	DAP_TCLK_SWCLK	JTAG_MUX_TCK FLEXIO1_FLEXIO30 **LPUART5_CTS_B**	GPIO3[30]	3rd UART Clear to Send no TX standard **input** signal
71	GND	GND				
Module Specific Signals						
72	3V3		SD1_DATA4	USDHC1_DATA4 FLEXSPI1_A_DATA04 FLEXIO1_FLEXIO14	GPIO3[14]	
73	3V3		SD1_DATA5	USDHC1_DATA5 FLEXSPI1_A_DATA05 USDHC1_RESET_B FLEXIO1_FLEXIO15	GPIO3[15]	
74	3V3		SD1_DATA6	USDHC1_DATA6 FLEXSPI1_A_DATA06 USDHC1_CD_B FLEXIO1_FLEXIO16	GPIO3[16]	
75	3V3		SD1_DATA7	USDHC1_DATA7 FLEXSPI1_A_DATA07 USDHC1_WP FLEXIO1_FLEXIO17	GPIO3[17]	
76	3V3	TXCAN	PDM_CLK	PDM_CLK, MQS1_LEFT LPTMR1_ALT1, **CAN1_TX**	GPIO1[8]	
77	3V3		CCM_CLKO1	CCMSRCGPCMIX_CLKO1 FLEXIO1_FLEXIO26	GPIO3[26]	
78	3V3		CCM_CLKO2	CCMSRCGPCMIX_CLKO2 FLEXIO1_FLEXIO27	GPIO3[27]	
79	3V3		CCM_CLKO3	CCMSRCGPCMIX_CLKO3 FLEXIO2_FLEXIO28	GPIO4[28]	
80	3V3		CCM_CLKO4	CCMSRCGPCMIX_CLKO4 FLEXIO2_FLEXIO29	GPIO4[29]	
81	3V3	RXCAN	PDM_BIT_STREAM0	PDM_BIT_STREAM00, MQS1_RIGHT LPSPI1_PCS1, TPM1_EXTCLK LPTMR1_ALT2, **CAN1_RX**	GPIO1[9]	
82	GND	GND				
83	Not connected					
84	Not connected					
85	Not connected					
86	Not connected					
87	Not connected					
88	GND	GND				

PIN	Type	TX Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
89	Not connected					
90	Not connected					
91	Not connected					
92	Not connected					
93	Not connected					
94	GND	GND				
95	Not connected					
96	Not connected					
97	Not connected					
98	Not connected					
99	Not connected					
100	Not connected					
101	Not connected					
102	GND	GND				
MISC						
103	3V3		ENET2_RXC	ENET1_RGMII_RXC, ENET1_RX_ER SAI2_TX_DATA01, FLEXIO2_FLEXIO23	GPIO4[23]	
104	3V3		ENET2_RX_CTL	ENET1_RGMII_RX_CTL LPUART4_DSR_B, SAI2_TX_DATA00 FLEXIO2_FLEXIO22	GPIO4[22]	
105	3V3		ENET2_TX_CTL	ENET1_RGMII_TX_CTL LPUART4_DTR_B, SAI2_TX_SYNC FLEXIO2_FLEXIO20	GPIO4[20]	
106	3V3		ENET2_RD1	ENET1_RGMII_RD1 SPDIF_IN, SAI2_TX_DATA03 FLEXIO2_FLEXIO25 of	GPIO4[25]	
107	3V3		ENET1_TD3	ENET_QOS_RGMII_TD3 CAN2_TX, HSIOMIX_OTG_ID2 FLEXIO2_FLEXIO02	GPIO4[2]	
108	3V3		ENET2_TD2	ENET1_RGMII_TD2 ENET1_TX_CLK, SAI2_RX_DATA01 FLEXIO2_FLEXIO17	GPIO4[17]	
109	3V3		ENET2_TD3	ENET1_RGMII_TD3 SAI2_RX_DATA00 FLEXIO2_FLEXIO16	GPIO4[16]	
110	3V3		ENET2_TXC	ENET1_RGMII_TXC ENET1_TX_ER, SAI2_TX_BCLK FLEXIO2_FLEXIO21	GPIO4[21]	
111	GND	GND				
112	3V3		SD3_DATA2	USDHC3_DATA2 FLEXSPI1_A_DATA02 FLEXIO1_FLEXIO24	GPIO3[24]	
113	3V3		ENET2_RD3	ENET1_RGMII_RD3 SPDIF_OUT, SPDIF_IN MQS2_LEFT, FLEXIO2_FLEXIO27	GPIO4[27]	
114	3V3		I2C2_SDA	LPI2C2_SDA, LPUART2_RIN_B TPM2_CH3, SAI1_RX_BCLK	GPIO1[3]	
115	3V3		SD1_STROBE	USDHC1_STROBE FLEXSPI1_A_DQS FLEXIO1_FLEXIO18	GPIO3[18]	
116	GND	GND				
Display						
117	3V3		GPIO_IO04	TPM3_CH0, PDM_CLK **MEDIAMIX_DISP_DATA00** LPSPI7_PCS0, LPUART6_TX LPI2C6_SDA, FLEXIO1_FLEXIO04	GPIO2[4]	
118	3V3		GPIO_IO05	TPM4_CH0 PDM_BIT_STREAM00 **MEDIAMIX_DISP_DATA01** LPSPI7_SIN, LPUART6_RX LPI2C6_SCL, FLEXIO1_FLEXIO05	GPIO2[5]	
119	3V3		GPIO_IO06	TPM5_CH0 PDM_BIT_STREAM01 **MEDIAMIX_DISP_DATA02** LPSPI7_SOUT, LPUART6_CTS_B LPI2C7_SDA, FLEXIO1_FLEXIO06	GPIO2[6]	

PIN	Type	TX Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
120	3V3		GPIO_IO07	LPSPI3_PCS1 MEDIAMIX_CAM_DATA01 **MEDIAMIX_DISP_DATA03** LPSPI7_SCK, LPUART6_RTS_B LPI2C7_SCL, FLEXIO1_FLEXIO07	GPIO2[7]	
121	3V3		GPIO_IO08	LPSPI3_PCS0 MEDIAMIX_CAM_DATA02 **MEDIAMIX_DISP_DATA04** TPM6_CH0, LPUART7_TX LPI2C7_SDA, FLEXIO1_FLEXIO08	GPIO2[8]	
122	3V3		GPIO_IO09	LPSPI3_SIN MEDIAMIX_CAM_DATA03 **MEDIAMIX_DISP_DATA05** TPM3_EXTCLK, LPUART7_RX LPI2C7_SCL, FLEXIO1_FLEXIO09	GPIO2[9]	
123	3V3		GPIO_IO10	LPSPI3_SOUT MEDIAMIX_CAM_DATA04 **MEDIAMIX_DISP_DATA06** TPM4_EXTCLK, LPUART7_CTS_B LPI2C8_SDA, FLEXIO1_FLEXIO10	GPIO2[10]	
124	3V3		GPIO_IO11	LPSPI3_SCK MEDIAMIX_CAM_DATA05 **MEDIAMIX_DISP_DATA07** TPM5_EXTCLK, LPUART7_RTS_B LPI2C8_SCL, FLEXIO1_FLEXIO11	GPIO2[11]	
125	3V3		GPIO_IO12	TPM3_CH2 PDM_BIT_STREAM02 **MEDIAMIX_DISP_DATA08** LPSPI8_PCS0, LPUART8_TX LPI2C8_SDA, SAI3_RX_SYNC	GPIO2[12]	
126	3V3		GPIO_IO13	TPM4_CH2 PDM_BIT_STREAM03 **MEDIAMIX_DISP_DATA09** LPSPI8_SIN, LPUART8_RX LPI2C8_SCL, FLEXIO1_FLEXIO13	GPIO2[13]	
127	3V3		GPIO_IO14	LPUART3_TX MEDIAMIX_CAM_DATA06 **MEDIAMIX_DISP_DATA10** LPSPI8_SOUT, LPUART8_CTS_B LPUART4_TX, FLEXIO1_FLEXIO14	GPIO2[14]	
128	3V3		GPIO_IO15	LPUART3_RX MEDIAMIX_CAM_DATA07 **MEDIAMIX_DISP_DATA11** LPSPI8_SCK, LPUART8_RTS_B LPUART4_RX, FLEXIO1_FLEXIO15	GPIO2[15]	
129	GND	GND				
130	3V3		GPIO_IO16	GPIO2_IO16, SAI3_TX_BCLK PDM_BIT_STREAM02 **MEDIAMIX_DISP_DATA12** LPUART3_CTS_B LPSPI4_PCS2, LPUART4_CTS_B FLEXIO1_FLEXIO16	GPIO2[16]	
131	3V3		GPIO_IO17	SAI3_MCLK MEDIAMIX_CAM_DATA08 **MEDIAMIX_DISP_DATA13** LPUART3_RTS_B, LPSPI4_PCS1 LPUART4_RTS_B, FLEXIO1_FLEXIO17	GPIO2[17]	
132	3V3		GPIO_IO18	SAI3_RX_BCLK MEDIAMIX_CAM_DATA09 **MEDIAMIX_DISP_DATA14** LPSPI5_PCS0, LPSPI4_PCS0 TPM5_CH2, FLEXIO1_FLEXIO18	GPIO2[18]	
133	3V3		GPIO_IO19	SAI3_RX_SYNC PDM_BIT_STREAM03 **MEDIAMIX_DISP_DATA15** LPSPI5_SIN, LPSPI4_SIN TPM6_CH2, SAI3_TX_DATA00	GPIO2[19]	
134	3V3		GPIO_IO20	SAI3_RX_DATA00 PDM_BIT_STREAM00 **MEDIAMIX_DISP_DATA16** LPSPI5_SOUT, LPSPI4_SOUT TPM3_CH1, FLEXIO1_FLEXIO20	GPIO2[20]	
135	3V3		GPIO_IO21	SAI3_TX_DATA00, PDM_CLK **MEDIAMIX_DISP_DATA17** LPSPI5_SCK, LPSPI4_SCK TPM4_CH1, SAI3_RX_BCLK	GPIO2[21]	
136	3V3		GPIO_IO22	USDHC3_CLK, SPDIF_IN **MEDIAMIX_DISP_DATA18** TPM5_CH1, TPM6_EXTCLK LPI2C5_SDA FLEXIO1_FLEXIO22	GPIO2[22]	
137	3V3		GPIO_IO23	USDHC3_CMD, SPDIF_OUT **MEDIAMIX_DISP_DATA19**	GPIO2[23]	

PIN	Type	TX Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
				TPM6_CH1, LPI2C5_SCL FLEXIO1_FLEXIO23		
138	3V3		GPIO_IO24	USDHC3_DATA0 **MEDIAMIX_DISP_DATA20** TPM3_CH3, JTAG_MUX_TDO LPSPI6_PCS1, FLEXIO1_FLEXIO24	GPIO2[24]	
139	3V3		GPIO_IO25	USDHC3_DATA1, CAN2_TX **MEDIAMIX_DISP_DATA21** TPM4_CH3, JTAG_MUX_TCK LPSPI7_PCS1, FLEXIO1_FLEXIO25	GPIO2[25]	
140	3V3		GPIO_IO26	USDHC3_DATA2 PDM_BIT_STREAM01 **MEDIAMIX_DISP_DATA22** TPM5_CH3, JTAG_MUX_TDI LPSPI8_PCS1, SAI3_TX_SYNC	GPIO2[26]	
141	3V3		GPIO_IO27	USDHC3_DATA3, CAN2_RX **MEDIAMIX_DISP_DATA23** TPM6_CH3, JTAG_MUX_TMS LPSPI5_PCS1, FLEXIO1_FLEXIO27	GPIO2[27]	
142	GND	GND				
143	3V3		GPIO_IO03	LPI2C4_SCL MEDIAMIX_CAM_HSYNC **MEDIAMIX_DISP_HSYNC** LPSPI6_SCK, LPUART5_RTS_B LPI2C6_SCL, FLEXIO1_FLEXIO03	GPIO2[3]	
144	3V3		GPIO_IO02	LPI2C4_SDA MEDIAMIX_CAM_VSYNC **MEDIAMIX_DISP_VSYNC** LPSPI6_SOUT, LPUART5_CTS_B LPI2C6_SDA, FLEXIO1_FLEXIO02	GPIO2[2]	
145	3V3		GPIO_IO01	LPI2C3_SCL MEDIAMIX_CAM_DATA00 **MEDIAMIX_DISP_DE** LPSPI6_SIN, LPUART5_RX LPI2C5_SCL, FLEXIO1_FLEXIO01	GPIO2[1]	
146	3V3		GPIO_IO00	LPI2C3_SDA MEDIAMIX_CAM_CLK **MEDIAMIX_DISP_CLK** LPSPI6_PCS0, LPUART5_TX LPI2C5_SDA, FLEXIO1_FLEXIO00	GPIO2[0]	
147	GND	GND				
Module Specific Signals						
148	3V3		ENET1_TXC	CCM_ENET_QOS_CLOCK_GENERATE_TX_CLK ENET_QOS_TX_ER FLEXIO2_FLEXIO07	GPIO4[7]	
149	3V3		PDM_BIT_STREAM1	PDM_BIT_STREAM01 NMI_GLUE_NMI, LPSPI2_PCS1 TPM2_EXTCLK, LPTMR1_ALT3 CCMSRCGPCMIX_EXT_CLK1	GPIO1[10]	
150	3V3		ENET2_MDC	ENET1_MDC, LPUART4_DCB_B SAI2_RX_SYNC, FLEXIO2_FLEXIO14	GPIO4[14]	
151	3V3		ENET2_MDIO	ENET1_MDIO, LPUART4_RIN_B SAI2_RX_BCLK, FLEXIO2_FLEXIO15	GPIO4[15]	
152	3V3		SD2_VSELECT	USDHC2_VSELECT, USDHC2_WP LPTMR2_ALT3, FLEXIO1_FLEXIO19 CCMSRCGPCMIX_EXT_CLK1	GPIO3[19]	
153	3V3		WDOG_ANY	WDOG1_WDOG_ANY	GPIO1[15] 10K-PU	Connected to PMIC WDOG_B
154	Not connected					
155	Not connected					
156	Not connected					
157	Not connected					
158	1V8 analog		CLKIN1		10K-PD	
159	1V8 analog		CLKIN2		10K-PD	
160	GND	GND				
161	1V8 analog		ADCIN0			
162	1V8 analog		ADCIN1			
163	1V8 analog		ADCIN2			
164	1V8		ADCIN3			

PIN	Type	TX Standard	i.MX91 Pad Name	Alternate functions	GPIO	Description (refer to i.MX 91 manuals for details)
	analog					
165	Not connected					
MIPI CSI						
166	MIPI		MIPI_CSI1_CLK_N			
167	MIPI		MIPI_CSI1_DATA1_N			
168	MIPI		MIPI_CSI1_CLK_P			
169	MIPI		MIPI_CSI1_DATA1_P			
170	MIPI		MIPI_CSI1_DATA0_N			
171	GND					
172	MIPI		MIPI_CSI1_DATA0_P			
173	1V8		TAMPER0			
174	1V8		TAMPER1			
175	Not connected					
176	Not connected					
177	Not connected					
178	Not connected					
179	Not connected					
180	Not connected					
181	Not connected					
182	Not connected					
183	GND					
184	Not connected					
185	Not connected					
186	Not connected					
187	Not connected					
188	Not connected					
189	Not connected					
190	Not connected					
191	Not connected					
192	Not connected					
193	Not connected					
194	Not connected					
195	Not connected					
196	Not connected					
197	Not connected					
198	Not connected					
199	Not connected					
200	GND					

Onboard peripherals wiring

USED FOR		i.MX 91 Pad Name	Alternate functions	GPIO	Description
		Refer to i.MX 91 manuals for details!			
eMMC	CMD	SD1_CMD	USDHC1_CMD	GPIO3[9]	
	CLK	SD1_CLK	USDHC1_CLK	GPIO3[8]	
	DAT0	SD1_DATA0	USDHC1_DATA0	GPIO3[10]	
	DAT1	SD1_DATA1	USDHC1_DATA1	GPIO3[11]	
	DAT2	SD1_DATA2	USDHC1_DATA2	GPIO3[12]	
	DAT3	SD1_DATA3	USDHC1_DATA3	GPIO3[13]	
PMIC	SDA	I2C1_SDA	I2C1_SDA	GPIO1[1]	10K-PU
	SCL	I2C1_SCL	I2C1_SCL	GPIO1[0]	1K-PU
	PMIC_ON_REQ	PMIC_ON_REQ			
	PMIC_STBY_REQ	PMIC_STBY_REQ			
	CLK_32K_OUT	RTC_XTALI			
ETHERNET LAN8710 RMII	MDC	ENET1_MDC	ENET_QOS_MDC	GPIO4[0]	
	MDIO	ENET1_MDIO	ENET_QOS_MDIO	GPIO4[1]	1K-PU
	RXD0	ENET1_RD0	ENET_QOS_RGMII_RD0	GPIO4[10]	
	RXD1	ENET1_RD1	ENET_QOS_RGMII_RD1	GPIO4[11]	
	RXER	ENET1_RXC	ENET_QOS_RX_ER	GPIO4[9]	
	TXEN	ENET1_TX_CTL	ENET_QOS_RGMII_TX_CTL	GPIO4[6]	
	TXD0	ENET1_TD0	ENET_QOS_RGMII_TD0	GPIO4[5]	
	TXD1	ENET1_TD1	ENET_QOS_RGMII_TD1	GPIO4[4]	
	COL/CRS_DV	ENET1_RX_CTL	ENET_QOS_RGMII_RX_CTL	GPIO4[8]	10K-PU
	nRST	ENET1_RD3		GPIO4[13]	10K-PU
	nINT	ENET1_RD2		GPIO4[12]	10K-PU
	XTAL1/CLKIN	ENET1_TD2	CCM_ENET_QOS_CLOCK_GENERATE_REF_CLK	GPIO4[3]	