TX51

Computer On Module

- Processor Freescale i.MX515, 800 MHz
- RAM 128/256MB mobile DDR-SDRAM
- ROM 128MB NAND Flash
- RTC DS1339 Real Time Clock
- Power supply Single 3.1V to 5.5V
- Size 26mm SO-DIMM
- Temp.-Range -20°C/0°C..70°C

800 MHz
Cortex A8

Key Features

- 10/100Mbps Ethernet
- Two High Speed USB 2.0 ports
- LCD controller up to 1280 x 768, 24bpp
- OpenGL ES 2.0 and OpenVG 1.1 hardware accelerators
- Multi-format HD 720p video decoder and D1 video encoder hardware engine
- Two Camera Interfaces
- NEON SIMD media accelerator
- Unified 256KB L2 cache
- Vector Floating Point Unit
- Several interfaces:
  3x UART, 2x SDIO, 2x SSI/AC97/I2S,
  I2C, CSPI, Keypad, Ext. Memory I/F

OS Support

- Windows Embedded CE
- Linux
- RedBoot Bootloader

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Board highlights:

- standard TX-DIMM pinout
- low power consumption
- as small as possible - only 26mm

The TX51 is a member of a module series, specially designed for Freescales i.MX multimedia processors. TX modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TX modules includes a Freescale® i.MX processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of an LCD screen. The TX51 is specifically targeted at embedded multimedia applications where size, high cpu-performance and low power consumption are critical factors. The i.MX515 multimedia applications processor offers high performance processing optimized for the lowest power consumption for smartbooks and netbooks. It features Freescale's advanced and power-efficient implementation of the ARM Cortex™-A8 core, which operates at speeds up to 800 MHz.

CPU Complex

- up to 800 MHz ARM Cortex-A8 CPU
- Unified 256KB L2 cache
- NEON SIMD media accelerator
- Vector floating point co-processor

Multimedia

- OpenGL ES 2.0 and OpenVG 1.1 hardware accelerators
- Multi-format HD 720p video decoder and D1 video encoder hardware engine
- 24-bit primary display support up to WXGA resolution
- Analog HD720p component TV output
- High quality hardware video de-interlacing
- Image and video resize, inversion, and rotation hardware
- Alpha blending and color space conversion
- Video/graphics combining: four planes & hardware cursor
- Display quality enhancement: color correction, gamut mapping, gamma correction

Standard TX-DIMM interface
Universal 1.8V Interfaces:

- 4-wire UART (x3)
- up to 24-bit LCD Interface
- I2C/Keypad
- SSI/AC97/I2S
- 4-wire SDIO (x2)
- Camera (x2)

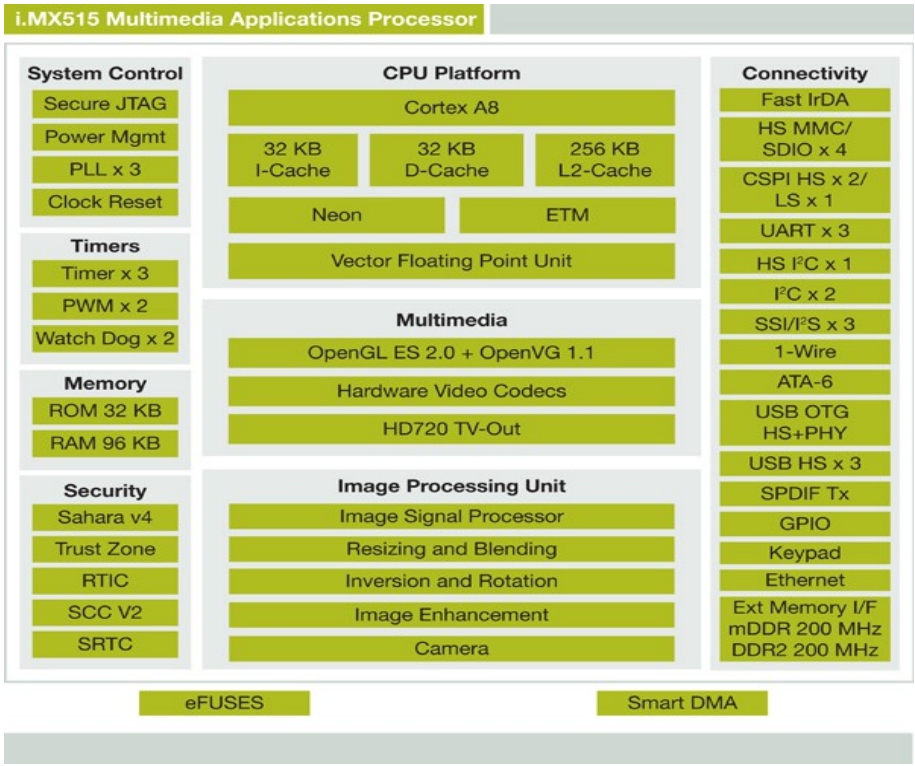
High-Speed communication interfaces incl. onboard PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- High Speed USB 2.0 OTG
- High Speed USB 2.0 Host

Power Supply
The TX51 accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (3.1V to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

1.8V and 3.3V power supply outputs of the TX51 can also be used on the baseboard.



Ordering Information

Order Number	i.MX515	SDRAM	Flash	Temp.
TX51/800/128S/128F	800MHz	128MB	128MB	-20°C..70°C
TX51/800/256S/128F	800MHz	256MB	128MB	0°C..70°C

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PIN	Type	Function	i.MX51 Pad Name	Alternate functions	GPIO/PU	Description (refer to i.MX51 manuals for details)
POWER SUPPLY & RESET						
1-4	power	VIN	-			Module power supply input (3.0V-5.5V)
5-7	power	1V8_OUT	-			1.8V buck regulator output, up to 300mA
8	1V8	BOOTMODE	-		10K-PU	Boot mode select H: Boot from NAND / L: Boot from UART/USB Leave unconnected or tie to 1V8, if not used.
9-12	power	3V3_OUT	-			3.3V buck regulator output, up to 1A
13	power	VBACKUP	-			DS1339 RTC backup power supply. Supply voltage must be held between 1.3V and 3.7V for proper RTC operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.
14	2.8V to 5.5V	PMIC_PWR_ON	-		10K-PD	This is an active high push button input which can be used to signal PWR_ON and PWR_OFF events to the CPU by controlling the PMIC ext_wakup signal and select contents of PMIC register 8H'88. Connected to a GPIO.
15	1V8	#RESET_OUT	EIM_A21		GPIO2_15	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controlled as a GPIO during runtime.
16	2V8	#PMIC_RESET_IN	-		10K-PU	Power On Reset—Active low input signal. Typically a push button reset or driven by an open collector output. Please refer to the PMIC datasheet for details. Leave unconnected, if not used.
17	1V8	#RESET_IN	RESET_IN_B		10K-PU	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset.
18	GND	GND				
Ethernet						
19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LINKLED				Active low LINK ON indication: Active indicates that the link is on.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_ACTLED				Active low ACTIVITY indication: Active indicates that there is Carrier sense (CRS) from the active PMD.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB-HOST						
27	3V3	USBH_VBUSEN				Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	GPIO1_6	SSI_EXT2_CLK	GPIO1_6 10K-PU	Active low over-current indicator input connected to a GPIO.
29	analog	USBH_DM				D- pin of the USB cable
30	analog	USBH_VBUS				VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
31	analog	USBH_DP				D+ pin of the USB cable
32	GND	GND				
USB-OTG						
33	3V3	USBOTG_ID	ID			ID pin of the USB cable. For an A-Device ID is grounded. For a B-Device ID is floated.
34	3V3	USBOTG_VBUSEN	GPIO1_8	USB_PWR / CLKO2 CSI2_DATA_EN ESDHC2_CD	GPIO1_8	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	analog	USBOTG_DM	DM			D- pin of the USB cable
36	3V3	#USBOTG_OC	GPIO1_9	USB_OC / CLKO DI2_D1_CS CCM_OUT_1 ESDHC2_LCTL	GPIO1_9 10K-PU	Active low over-current indicator input connected to a GPIO.
37	analog	USBOTG_DP	DP			D+ pin of the USB cable
38	analog	USBOTG_VBUS	VBUS			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.

PIN	Type	Function	i.MX51 Pad Name	Alternate functions	GPIO/PU	Description (refer to i.MX51 manuals for details)
39	GND	GND				
I2C						
40	1V8	I2C_DATA	EIM_D24	**I2C2_SDA** UART3_CTS AUD6_RXFS	GPIO2_8	I2C Data
41	1V8	I2C_CLK	EIM_D27	**I2C2_SCL** UART3_RTS AUD6_RXC	GPIO2_9	I2C Clock
PWM						
42	**3V1**	PWM	GPIO1_2	PWM1_PWMO I2C2_SCL CCM_OUT_2	GPIO1_2	**Be aware of the voltage level on this pin!**
1-WIRE						
43	1V8	OWIRE	OWIRE_LINE	SPDIF_OUT1	GPIO1_24	
CSPI – Configurable Serial Peripheral Interface						
44	1V8	CSPI_SS0	CSPI1_SS0	AUD4_TXC	GPIO4_24	Slave Select (Selectable polarity) signal
45	1V8	CSPI_SS1	CSPI1_SS1	AUD4_TXD	GPIO4_25	Slave Select (Selectable polarity) signal
46	1V8	CSPI_MOSI	CSPI1_MOSI	I2C1_SDA	GPIO4_22	Master Out/Slave In signal
47	1V8	CSPI_MISO	CSPI1_MISO	AUD4_RXD	GPIO4_23	Master In/Slave Out signal
48	1V8	CSPI_SCLK	CSPI1_SCLK	I2C1_SCL	GPIO4_27	Serial Clock signal
49	1V8	CSPI_RDY	CSPI1_RDY	AUD4_TXFS	GPIO4_26	Serial Data Ready signal
50	GND	GND				
SD – Secure Digital Interface 1						
51	1V8	SD1_CD	DISPB2_SER_RS	VALID_ESC_IN DI1_PIN16 DI1_PIN8	GPIO3_8	SD Card Detect – connected to a GPIO
52	1V8	SD1_D[0]	SD1_DATA0	AUD5_TXD CSPI_MISO	-	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	1V8	SD1_D[1]	SD1_DATA1	AUD5_RXD	-	
54	1V8	SD1_D[2]	SD1_DATA2	AUD5_TXC	-	
55	1V8	SD1_D[3]	SD1_DATA3	AUD5_TXFS CSPI_SS1	-	
56	1V8	SD1_CMD	SD1_CMD	AUD5_RXFS CSPI_MOSI	-	SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4. 7K–69 K external pull up resistor must be added.
57	1V8	SD1_CLK	SD1_CLK	AUD5_RXC CSPI_SCLK	-	SD Output Clock.
58	GND	GND				
UART1						
59	1V8	UART1_TXD	UART1_TXD	PWM2_PWMO REQUEST_ESC_OUT	GPIO4_29	Transmit Data output signal
60	1V8	UART1_RXD	UART1_RXD	READY_ESC_OUT	GPIO4_28	Receive Data input signal
61	1V8	UART1_RTS	UART1_RTS	CLK_ESC_OUT	GPIO4_30	Request to Send input signal
62	1V8	UART1_CTS	UART1_CTS	READY_HS_OUT	GPIO4_31	Clear to Send output signal
UART2						
63	1V8	UART2_TXD	UART2_TXD	FIRI_RXD VALID_ESC_OUT	GPIO1_21	Transmit Data output signal
64	1V8	UART2_RXD	UART2_RXD	FIRI_TXD VALID_HS_OUT	GPIO1_20	Receive Data input signal
65	1V8	UART2_RTS	EIM_D26	KPP_COL[7] UART3_TXD_MUX **UART2_RTS** CMPOUT2	-	Request to Send input signal
66	1V8	UART2_CTS	EIM_D25	KPP_COL[6] UART3_RXD_MUX **UART2_CTS** CMPOUT1	-	Clear to Send output signal

PIN	Type	Function	i.MX51 Pad Name	Alternate functions	GPIO/PU	Description (refer to i.MX51 manuals for details)
UART3						
67	1V8	UART3_TXD	UART3_TXD	UART1_DSR CSI1_D[1] REQUEST_HS_OUT	GPIO1_23	Transmit Data output signal
68	1V8	UART3_RXD	UART3_RXD	UART1_DTR CSI1_D[0] SYNC_HS_OUT	GPIO1_22	Receive Data input signal
69	1V8	UART3_RTS	EIM_D18	UART2_TXD_MUX **UART3_RTS** AUD5_TXC	GPIO2_2	Request to Send input signal
70	1V8	UART3_CTS	EIM_D17	UART2_RXD_MUX **UART3_CTS** AUD5_RXD	GPIO2_1	Clear to Send output signal
71	GND	GND				
KEYPAD						
72	1V8	KP_COL[0]	KEY_COL0	CSU_ALARM_AUT[1] HS_TX_E0	-	Keypad Column selection signals.
73	1V8	KP_COL[1]	KEY_COL1	CSU_ALARM_AUT[2] HS_TX_E1	-	
74	1V8	KP_COL[2]	KEY_COL2		-	
75	1V8	KP_COL[3]	KEY_COL3		-	
76	1V8	KP_COL[4]	KEY_COL4	UART1_RI UART3_RTS I2C2_SCL SSI_EXT2_CLK SPDIF_OUT1	-	
77	1V8	KP_ROW[0]	KEY_ROW0	EMI_DSTROBE SCC_RANDOM_V	-	Keypad Row selection signals.
78	1V8	KP_ROW[1]	KEY_ROW1	RTIC_SEC_VIO SCC_RANDOM	-	
79	1V8	KP_ROW[2]	KEY_ROW2	RTIC_DONE_INT SJC_DONE	-	
80	1V8	KP_ROW[3]	KEY_ROW3	CSU_ALARM_AUT[0] SJC_FAIL	-	
81	1V8	KP_COL[5]	KEY_COL5	UART1_DCD UART3_CTS I2C2_SDA SSI_EXT1_CLK MCT_EXT_ACT_TRIG	-	
82	GND	GND				
SSI 1 - Serial Audio Port 1						
83	1V8	SSI1_INT	DI1_D0_CS	LPDT_ESC_IN	GPIO3_3	GPIO
84	1V8	SSI1_RXD	AUD3_BB_RXD	UART3_RXD_MUX	GPIO4_19	Receive serial data
85	1V8	SSI1_TXD	AUD3_BB_TXD	SLM_DATA	GPIO4_18	Transmit serial data
86	1V8	SSI1_CLK	AUD3_BB_CK	SLM_CLK	GPIO4_20	Serial clock
87	1V8	SSI1_FS	AUD3_BB_FS	UART3_TXD_MUX	GPIO4_21	Frame Sync
88	GND	GND				
SSI 2 - Serial Audio Port 2						
89	1V8	SSI2_INT	DI1_D1_CS	READY_HS_IN DI1_PIN14 DI1_PIN5	GPIO3_4	GPIO
90	1V8	SSI2_RXD	EIM_D29	KPP_ROW[5] **AUD6_RXD**	-	Receive serial data
91	1V8	SSI2_TXD	EIM_D28	KPP_ROW[4] **AUD6_TXD**	-	Transmit serial data
92	1V8	SSI2_CLK	EIM_D30	KPP_ROW[6] **AUD6_TXC**	-	Serial clock
93	1V8	SSI2_FS	EIM_D31	KPP_ROW[7] **AUD6_TXFS**	-	Frame Sync
94	GND	GND				
Secure Digital Interface 2						
95	1V8	SD2_CD	DISPB2_SER_DIO	ACTIVE_HS_IN DI1_PIN6	GPIO3_6	SD Card Detect - connected to a GPIO

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				WDOG1_RST_B_DEB		
96	1V8	SD2_D[0]	SD2_DATA0	ESDHC1_DAT4 CSPI_MISO	-	SD Data bidirectional signals.
97	1V8	SD2_D[1]	SD2_DATA1	ESDHC1_DAT5 USBOH3_H2_DP	-	
98	1V8	SD2_D[2]	SD2_DATA2	ESDHC1_DAT6 USBOH3_H2_DM	-	
99	1V8	SD2_D[3]	SD2_DATA3	ESDHC1_DAT7 CSPI_SS2	-	
100	1V8	SD2_CMD	SD2_CMD	I2C1_SCL CSPI_MOSI	-	SD Command bidirectional signal.
101	1V8	SD2_CLK	SD2_CLK	I2C1_SDA CSPI_SCLK	-	SD Output Clock signal.
102	GND	GND				
CMOS Sensor Interface						
103	1V8	CSI_D0	CSI1_D12		-	Sensor port data
104	1V8	CSI_D1	CSI1_D13		-	Sensor port data
105	1V8	CSI_D2	CSI1_D14		-	Sensor port data
106	1V8	CSI_D3	CSI1_D15		-	Sensor port data
107	1V8	CSI_D4	CSI1_D16		-	Sensor port data
108	1V8	CSI_D5	CSI1_D17		-	Sensor port data
109	1V8	CSI_D6	CSI1_D18		-	Sensor port data
110	1V8	CSI_D7	CSI1_D19		-	Sensor port data
111	GND	GND				
112	1V8	CSI_HSYNC	CSI1_HSYNC		GPIO3_15	Sensor port horizontal sync
113	1V8	CSI_VSYNC	CSI1_VSYNC		GPIO3_14	Sensor port vertical sync
114	1V8	CSI_PIXCLK	CSI1_PIXCLK		-	Sensor port data latch clock
115	1V8	CSI_MCLK	CSI1_MCLK		-	Sensor port master clock
116	GND	GND				
LCD Controller						
117	1V8	LD0	DISP1_DAT0		-	LCD Data Bus
118	1V8	LD1	DISP1_DAT1		-	LCD Data Bus
119	1V8	LD2	DISP1_DAT2		-	LCD Data Bus
120	1V8	LD3	DISP1_DAT3		-	LCD Data Bus
121	1V8	LD4	DISP1_DAT4		-	LCD Data Bus
122	1V8	LD5	DISP1_DAT5		-	LCD Data Bus
123	1V8	LD6	DISP1_DAT6		-	LCD Data Bus
124	1V8	LD7	DISP1_DAT7		-	LCD Data Bus
125	1V8	LD8	DISP1_DAT8		-	LCD Data Bus
126	1V8	LD9	DISP1_DAT9		-	LCD Data Bus
127	1V8	LD10	DISP1_DAT10		-	LCD Data Bus
128	1V8	LD11	DISP1_DAT11		-	LCD Data Bus
129	GND	GND				

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130	1V8	LD12	DISP1_DAT12		-	LCD Data Bus
131	1V8	LD13	DISP1_DAT13		-	LCD Data Bus
132	1V8	LD14	DISP1_DAT14		-	LCD Data Bus
133	1V8	LD15	DISP1_DAT15		-	LCD Data Bus
134	1V8	LD16	DISP1_DAT16		-	LCD Data Bus
135	1V8	LD17	DISP1_DAT17		-	LCD Data Bus
136	1V8	LD18	DISP1_DAT18	DI2_PIN5 DI2_PIN11	-	LCD Data Bus
137	1V8	LD19	DISP1_DAT19	DI2_PIN6 DI2_PIN12	-	LCD Data Bus
138	1V8	LD20	DISP1_DAT20	DI2_PIN7 DI2_PIN13	-	LCD Data Bus
139	1V8	LD21	DISP1_DAT21	DI2_PIN8 DI2_PIN14	-	LCD Data Bus
140	1V8	LD22	DISP1_DAT22	DISP2_DAT[16] DI2_D0_CS	-	LCD Data Bus
141	1V8	LD23	DISP1_DAT23	DISP2_DAT[17] DI2_D1_CS	-	LCD Data Bus
142	GND	GND				
143	1V8	HSYNC	DI1_PIN2		-	Line Pulse or HSync
144	1V8	VSYNC	DI1_PIN3		-	Frame Sync or Vsync
145	1V8	OE_ACD	DI1_PIN15		-	Alternate Crystal Direction/Output Enable
146	1V8	LSCLK	DI1_DISP_CLK		-	Shift Clock
147	GND	GND				
Module Specific Signals						
148	**3V1**	CSI2_MCLK	GPIO1_5	WDOG_B DI2_PIN16 CLKO CSI2_MCLK	GPIO1_5	**Be aware of the voltage level on this pin!**
149	1V8	CSI2_PIXCLK	CSI2_PIXCLK	RX_BYTE_CLK_HS_O	GPIO4_15	
150	1V8	CSI2_VSYNC	CSI2_VSYNC	HS_RX_E	GPIO4_13	
151	1V8	CSI2_HSYNC	CSI2_HSYNC	TX_BYTE_CLK_HS_O	GPIO4_14	
152	1V8	CSI2_D12	CSI2_D12	LP_RX_E	GPIO4_9	
153	1V8	CSI2_D13	CSI2_D13	RX_VALID_ESC_OUT	GPIO4_10	
154	1V8	CSI2_D14	CSI2_D14		-	
155	1V8	CSI2_D15	CSI2_D15		-	
156	1V8	CSI2_D16	CSI2_D16		-	
157	1V8	CSI2_D17	CSI2_D17		-	
158	1V8	CSI2_D18	CSI2_D18	HS_TX_E	GPIO4_11	
159	1V8	CSI2_D19	CSI2_D19	LP_TX_E	GPIO4_12	
160	GND	GND				
161	1V8		CSI1_D8	DETECT_Z	GPIO3_12	
162	1V8		CSI1_D9	DELAY_Z	GPIO3_13	
163	1V8		CSI1_D10		-	
164	1V8		CSI1_D11		-	
165	1V8		DISPB2_SER_CLK	DI1_PIN17 DI1_PIN7 WDOG2_RST_B_DEB	GPIO3_7	
166	1V8		DISPB2_SER_DIN	VALID_HS_IN DI1_PIN1	GPIO3_5	

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167	1V8		CKIH1			
168	analog		TV_IOB			
169	analog		TV_IOG			
170	analog		TV_IOR			
171	GND	GND				
172	power		PMIC_VIN_BUBAT			Connected to PMIC
External Memory Interface						
173	1V8		EIM_CS0		GPIO2_25	
174	1V8		EIM_CS1		GPIO2_26	
175	1V8		EIM_DTACK		GPIO2_31	
176	1V8		EIM_WAIT		-	
177	1V8		EIM_EB0	DETECT_D	-	
178	1V8		EIM_EB1	DELAY_D	-	
179	1V8		EIM_OE		GPIO2_24	
180	1V8		EIM_LBA		GPIO3_1	
181	1V8		EIM_RW		-	
182	1V8		EIM_BCLK		-	
183	GND	GND				
184	1V8		EIM_DA0		-	
185	1V8		EIM_DA1		-	
186	1V8		EIM_DA2		-	
187	1V8		EIM_DA3		-	
188	1V8		EIM_DA4		-	
189	1V8		EIM_DA5		-	
190	1V8		EIM_DA6		-	
191	1V8		EIM_DA7		-	
192	1V8		EIM_DA8		-	
193	1V8		EIM_DA9		-	
194	1V8		EIM_DA10		-	
195	1V8		EIM_DA11		-	
196	1V8		EIM_DA12		-	
197	1V8		EIM_DA13		-	
198	1V8		EIM_DA14		-	
199	1V8		EIM_DA15		-	
200	GND	GND				