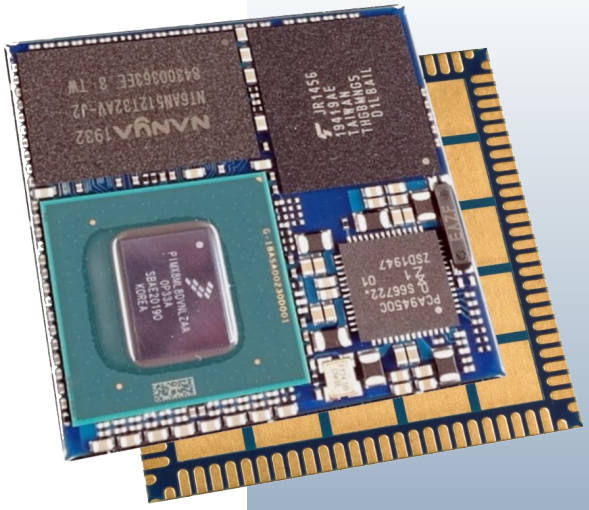
QSX-Series - QFN Style Solder-Down Computer On Module

NEW

- QSX – extended 2nd generation QS module series
- QS pin-compatible solder-down version
- 29mm square
- 2.6mm total height
- QFN type lead style
  - 1mm pitch
  - 108 pads
  - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- 3.3V-5V power supply (-5%/+10%)



Key Features

- NXP i.MX 8M Plus — Quad Cortex-A53 up to 1.6 GHz, Cortex-M7 up to 800 MHz
- RAM — 2 GB LPDDR4
- ROM — 8 GB eMMC
- Grade — Industrial
- Temperature — -30°C to 85°C
- Display support
  - MIPI DSI (4-lane)
  - GC520L 2D GPU
  - GC7000UL 3D GPU
  - 1080p60 video de-/encode
- Vision and Machine Learning
  - 2x MIPI-CSI (4-lane each)
  - Dual Camera ISP (2x HD/1x 12MP) HDR, dewarp
  - Machine Learning Accelerator: 2.3 TOPS
  - Tensilica® HiFi4 DSP up to 800 MHz
- Connectivity
  - 1x USB 3.0, 1x USB 2.0
  - 1x Gb Ethernet with IEEE®1588, AVB, TSN
  - 1x eMMC/SD, 2x CAN-FD
  - 1x PCIe® Gen 3 – 1-lane
  - 3x UART, 2x I²C, 2x SPI, PWM, SAI
  - Up to 60x 3.3V General Purpose I/O

i.MX 8M Plus

OS Support

- Linux

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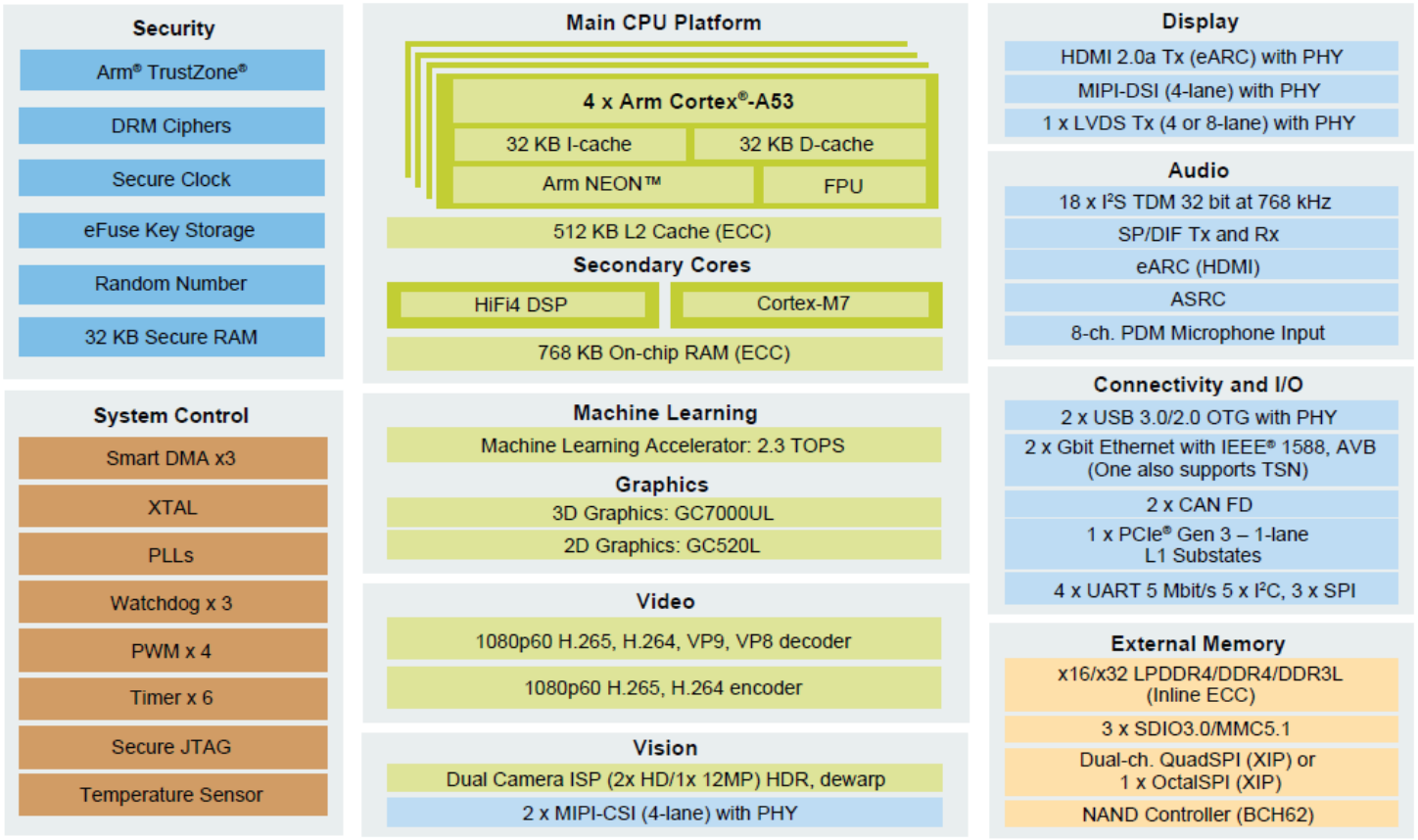
i.MX 8M Plus Block Diagram



QS8M – QSXM – QSXP – Differentiated Features and Ordering Information

	QS8M - i.MX 8M Mini	**QSXM** - i.MX 8M Mini	**QSXP** - i.MX 8M Plus
Primary Arm® Core	4x Cortex®-A53 1.6 GHz		
Secondary Arm® Core	Cortex-M4 400 MHz		Cortex-M7 800 MHz
RAM	1 GB DDR3L x16	2 GB LPDDR4 x32	
ROM	4 GB eMMC		8 GB eMMC
3D GPU	GCNanoUltra (1 shader, OpenGL ES 2.0)		GC7000UL (2 shaders, OpenGL ES 2.0/3.0/3.1 OpenCL 1.2, Vulkan)
2D GPU	GC520L		
AI/ML/DSP	-		NN Accel 2.3 TOPS Hi-Fi4 DSP 800 MHz
Video De-/Encode	1080p60 H.264		1080p60 H.264, H.265
Connectivity	2x USB 2.0	2x USB 2.0, PCIe	USB 2.0, USB 3.0, PCIe
QS Size	100 pins 27mm square	108 pins 29mm square	
Grade / Temperature	Industrial -25°C to 85°C	Industrial -30°C to 85°C	
Ordering Information	QS8M/MQ/1GS/4GF/E85	QSXM/MM6C/2GS/4GF/E85	QSXP/ML8C/2GS/8GF/E85

2021-04-09

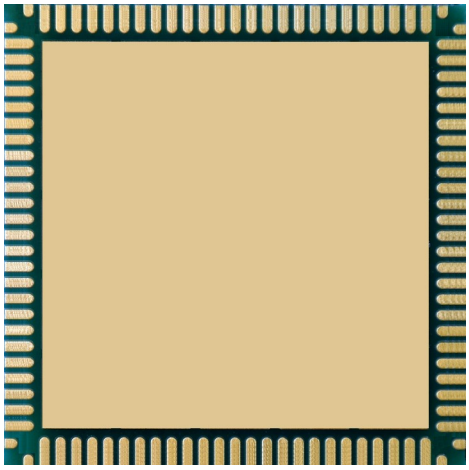
QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He also has to provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QS series of modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.



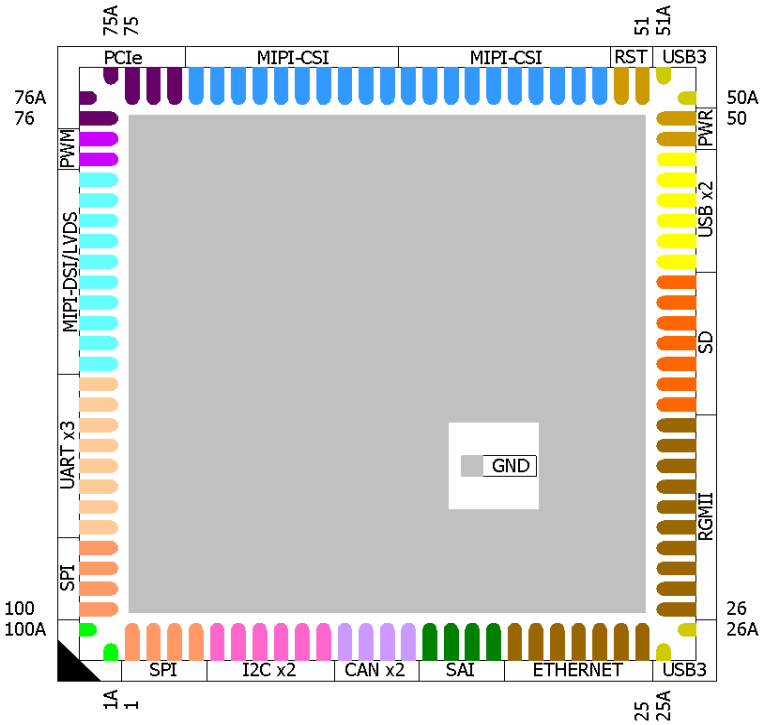
Easy Wiring - Even 2-layer printed circuit boards can be used.

With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing other routes.

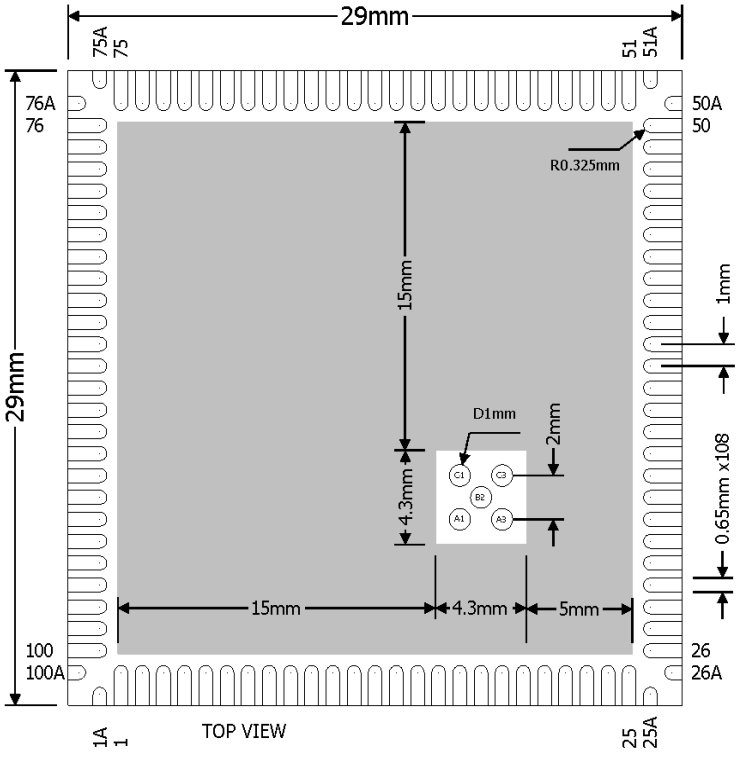
Advanced Soldering

Using a large solder pad underneath the component has not only electrical and thermal advantages. It is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight of the components, which could result in short circuits.

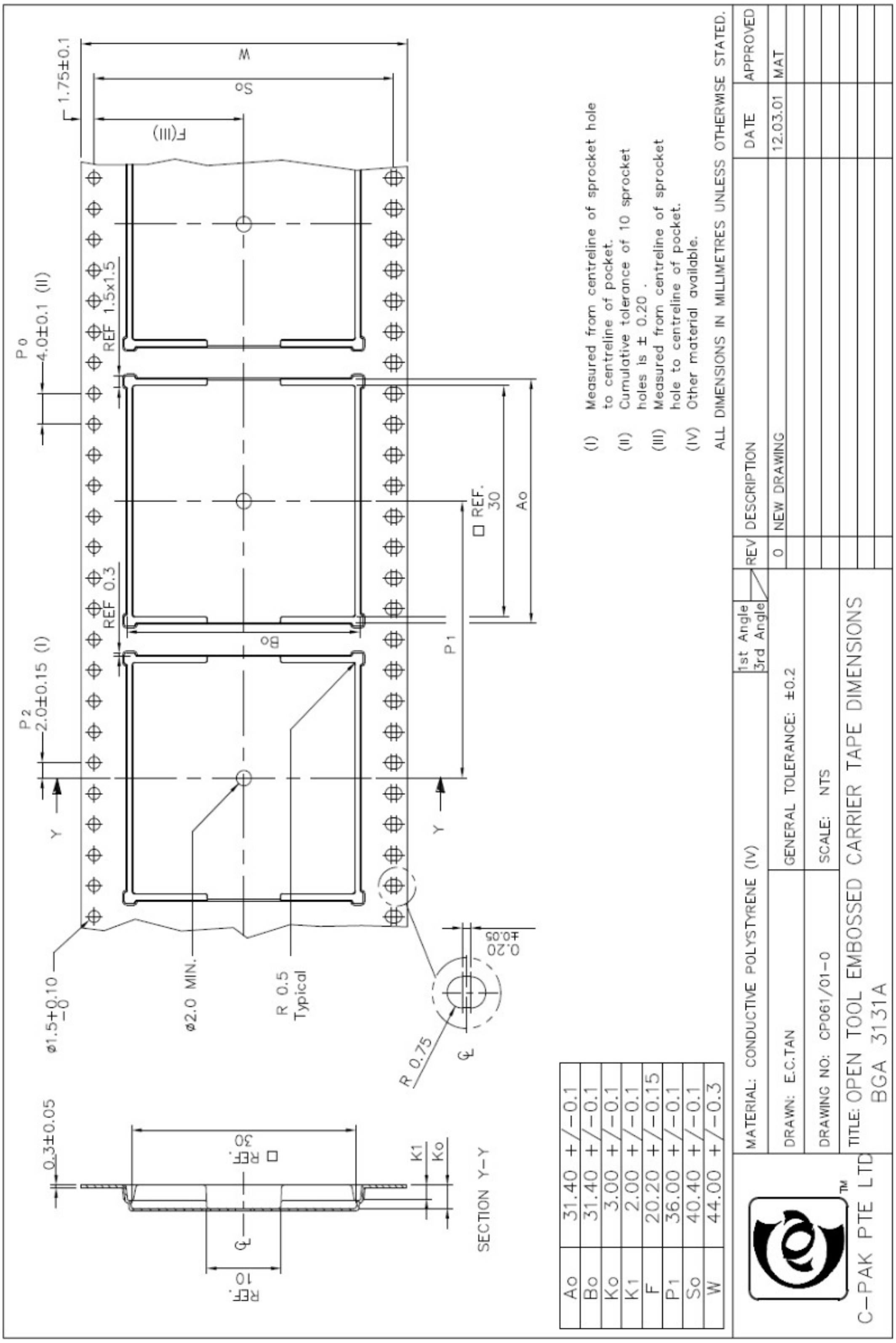
Standard Contact Assignments



Package Information



Packaging


W
So
F(III)
1.75±0.1
Po
4.0±0.1 (II)
REF 1.5x1.5
REF 0.3
P2
2.0±0.15 (I)
Y
Bo
P1
□ REF. 30
Ao
ø1.5+0.10 -0
ø2.0 MIN.
R 0.5 Typical
R 0.75
0.20 ±0.05
0.3±0.05
REF. 10
□ REF. 30
K1
Ko
SECTION Y-Y
Ao 31.40 +/-0.1
Bo 31.40 +/-0.1
Ko 3.00 +/-0.1
K1 2.00 +/-0.1
F 20.20 +/-0.15
P1 36.00 +/-0.1
So 40.40 +/-0.1
W 44.00 +/-0.3
(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.
REV DESCRIPTION DATE APPROVED
0 NEW DRAWING 12.03.01 MAT
1st Angle
3rd Angle
MATERIAL: CONDUCTIVE POLYSTYRENE (IV)
DRAWN: E.C.TAN
GENERAL TOLERANCE: ±0.2
DRAWING NO: CP061/01-0
SCALE: NTS
TITLE: OPEN TOOL EMBOSSED CARRIER TAPE DIMENSIONS
BGA 3131A
C-PAK PTE LTD
THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO C-PAK PTE.LTD.

Pinout

PIN	TYPE	QS-STANDARD	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description
			Refer to i.MX8M Plus manuals for details!			
1st SPI						
1	3V3	SPI_NSS_A	ECSPI2_SS0	UART4_RTS_B I2C4_SDA CCM_CLKO2	GPIO5[13]	
2	3V3	SPI_MISO_A	ECSPI2_MISO	UART4_CTS_B I2C4_SCL mux SAI7_MCLK CCM_CLKO1	GPIO5[12]	
3	3V3	SPI_MOSI_A	ECSPI2_MOSI	UART4_TX I2C3_SDA SAI7_TX_DATA[0]	GPIO5[11]	
4	3V3	SPI_SCK_A	ECSPI2_SCLK	UART4_RX I2C3_SCL SAI7_TX_BCLK	GPIO5[10]	
I2C						
5	3V3	I2C_SCL_A	I2C2_SCL	ENET_QOS_1588_EVENT1_IN USDHC3_CD_B ECSPI1_MISO ENET_QOS_1588_EVENT1_AUX_IN	GPIO5[16]	
6	3V3	I2C_SDA_A	I2C2_SDA	ENET_QOS_1588_EVENT1_OUT USDHC3_WP ECSPI1_SS0	GPIO5[17]	
7	3V3	INT_A	I2C4_SCL	PWM2_OUT PCIE_CLKREQ_B ECSPI2_MISO	GPIO5[20]	
8	3V3	I2C_SCL_B	I2C3_SCL	PWM4_OUT GPT2_CLK ECSPI2_SCLK	GPIO5[18]	
9	3V3	I2C_SDA_B	I2C3_SDA	PWM3_OUT GPT3_CLK ECSPI2_MOSI	GPIO5[19]	
10	3V3	INT_B	I2C4_SDA	PWM1_OUT ECSPI2_SS0	GPIO5[21]	
CAN						
11	3V3	CAN_RX_A	SPDIF_RX	SPDIF_IN PWM2_OUT I2C5_SDA GPT1_COMPARE2 **CAN1_RX**	GPIO5[04]	
12	3V3	CAN_TX_A	SPDIF_TX	SPDIF_OUT PWM3_OUT I2C5_SCL GPT1_COMPARE1 **CAN1_TX**	GPIO5[03]	
13	3V3	CAN_RX_B	SAI5_MCLK	SAI5_MCLK SAI1_TX_BCLK PWM1_OUT I2C5_SDA **CAN2_RX**	GPIO3[25]	
14	3V3	CAN_TX_B	SAI5_RXD3	SAI5_RX_DATA[3] SAI1_TX_DATA[5] SAI1_TX_SYNC SAI5_TX_DATA[0] BIT_STREAM[3] **CAN2_TX**	GPIO3[24]	
SAI						
15	3V3	SAI_TX	SAI2_TXD0	AUDIOMIX_SAI2_TX_DATA[0] AUDIOMIX_SAI5_TX_DATA[3] ENET_QOS_1588_EVENT2_IN CAN2_TX ENET_QOS_1588_EVENT2_AUX_IN SRC_BOOT_MODE[4]	GPIO4[26]	
16	3V3	SAI_RX	SAI2_RXD0	SAI2_RX_DATA[0] SAI5_TX_DATA[0] ENET_QOS_1588_EVENT2_OUT SAI2_TX_DATA[1] UART1_RTS_B BIT_STREAM[3]	GPIO4[23]	
17	3V3	SAI_SCK	SAI2_TXC	SAI2_TX_BCLK SAI5_TX_DATA[2] CAN1_RX BIT_STREAM[1]	GPIO4[25]	

PIN	TYPE	QS-STANDARD	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description
			Refer to i.MX8M Plus manuals for details!			
18	3V3	SAI_FS	SAI2_TXFS	SAI2_TX_SYNC SAI5_TX_DATA[1] ENET_QOS_1588_EVENT3_OUT AUDIOMIX_SAI2_TX_DATA[1] UART1_CTS_B AUDIOMIX_BIT_STREAM[2]	GPIO4[24]	
ETHERNET						
19	3V3	ENET_RST	SAI2_RXC	SAI2_RX_BCLK SAI5_TX_BCLK UART1_RX BIT_STREAM[1]	GPIO4[22]	
20	3V3	ENET_CK125	GPIO1_IO00	CCM_ENET_PHY_REF_CLK_ROOT ISP_FL_TRIG_0 CCM_EXT_CLK1	GPIO1[00]	
21	3V3	ENET_INT	SAI2_RXFS	SAI2_RX_SYNC SAI5_TX_SYNC SAI5_TX_DATA[1] SAI2_RX_DATA[1] UART1_TX AUDIOMIX_BIT_STREAM[2]	GPIO4[21]	
22	3V3 LDO5*)	ENET_MDIO	ENET_MDIO	SAI6_TX_SYNC BIT_STREAM[3] USDHC3_DATA5	GPIO1[17]	
23	3V3 LDO5*)	ENET_MDC	ENET_MDC	ENET_QOS_MDC SAI6_TX_DATA[0] USDHC3_STROBE	GPIO1[16]	
24	3V3 LDO5*)	ENET_RXC	ENET_RXC	CCM_ENET_QOS_CLOCK_ GENERATE_RX_CLK ENET_QOS_RX_ER SAI7_TX_BCLK BIT_STREAM[2] USDHC3_DATA3	GPIO1[25]	For RMII—ENET_RXC works as RMII.RX_ERR For RGMII—ENET_RXC works as RGMII.RX_CLK
25	3V3 LDO5*)	ENET_RX_CTL	ENET_RX_CTL	ENET_QOS_RGMII_RX_CTL SAI7_TX_SYNC BIT_STREAM[3] USDHC3_DATA2	GPIO1[24]	RMII.RX_EN (CRS_DV); RGMII.RC_CTL
26	3V3 LDO5*)	ENET_RXD0	ENET_RD0	ENET_QOS_RGMII_RD0 SAI7_RX_DATA[0] BIT_STREAM[1] USDHC3_DATA4	GPIO1[26]	RMII and RGMII.RD0
27	3V3 LDO5*)	ENET_RXD1	ENET_RD1	ENET_QOS_RGMII_RD1 SAI7_RX_SYNC BIT_STREAM[0] USDHC3_RESET_B	GPIO1[27]	RMII and RGMII.RD1
28	3V3 LDO5*)	ENET_RXD2	ENET_RD2	ENET_QOS_RGMII_RD2 SAI7_RX_BCLK AUDIOMIX_CLK USDHC3_CLK	GPIO1[28]	Only used for RGMII
29	3V3 LDO5*)	ENET_RXD3	ENET_RD3	ENET_QOS_RGMII_RD3 SAI7_MCLK SPDIF_IN USDHC3_CMD	GPIO1[29]	Only used for RGMII
30	3V3 LDO5*)	ENET_TX_CTL	ENET_TX_CTL	ENET_QOS_RGMII_TX_CTL SAI6_MCLK SPDIF_OUT USDHC3_DATA0	GPIO1[22]	RMII.TX_EN; RGMII.TX_CTL
31	3V3 LDO5*)	ENET_TXC	ENET_TXC	CCM_ENET_QOS_CLOCK_ GENERATE_TX_CLK ENET_QOS_TX_ER SAI7_TX_DATA[0] USDHC3_DATA1	GPIO1[23]	For RMII—ENET_TXC works as RMII.TX_ERR For RGMII—ENET_TXC works as RGMII.TX_CLK
32	3V3 LDO5*)	ENET_TXD3	ENET_TD3	ENET_QOS_RGMII_TD3 SAI6_TX_BCLK BIT_STREAM[2] USDHC3_DATA6	GPIO1[18]	Only used for RGMII
33	3V3 LDO5*)	ENET_TXD2	ENET_TD2	ENET_QOS_RGMII_TD2 CCM_ENET_QOS_CLOCK_ GENERATE_REF_CLK SAI6_RX_DATA[0] BIT_STREAM[1] USDHC3_DATA7	GPIO1[19]	Used as RMII clock and RGMII data, there are two RGMII clock schemes. • MAC generate output 50M reference clock for PHY, and MAC also use this 50M clock. • MAC use external 50M clock.
34	3V3 LDO5*)	ENET_TXD1	ENET_TD1	ENET_QOS_RGMII_TD1 SAI6_RX_SYNC BIT_STREAM[0] USDHC3_CD_B	GPIO1[20]	RMII and RGMII.TD1
35	3V3 LDO5*)	ENET_TXD0	ENET_TD0	ENET_QOS_RGMII_TD0 SAI6_RX_BCLK AUDIOMIX_CLK USDHC3_WP	GPIO1[21]	RMII and RGMII.TD0

PIN	TYPE	QS-STANDARD	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description
			Refer to i.MX8M Plus manuals for details!			
SD						
36	3V3	SD_CD	SD2_CD_B	USDHC2_CD_B	GPIO2[12]	
37	3V3	SD_D1	SD2_DATA1	USDHC2_DATA1 I2C4_SCL UART2_TX BIT_STREAM[1]	GPIO2[16]	
38	3V3	SD_D0	SD2_DATA0	USDHC2_DATA0 I2C4_SDA UART2_RX BIT_STREAM[0]	GPIO2[15]	
39	3V3	SD_CLK	SD2_CLK	USDHC2_CLK ECSPI2_SCLK UART4_RX	GPIO2[13]	
40	3V3	SD_CMD	SD2_CMD	USDHC2_CMD ECSPI2_MOSI UART4_TX AUDIOMIX_CLK	GPIO2[14]	
41	3V3	SD_D3	SD2_DATA3	USDHC2_DATA3 ECSPI2_MISO SPDIF_IN BIT_STREAM[3] SRC_EARLY_RESET	GPIO2[18]	
42	3V3	SD_D2	SD2_DATA2	USDHC2_DATA2 ECSPI2_SS0 SPDIF_OUT BIT_STREAM[2]	GPIO2[17]	
USB						
43	PHY	USBH_VBUS	USB2_VBUS			
44	PHY	USBH_DN	USB2_D_N			
45	PHY	USBH_DP	USB2_D_P			
46	PHY	USBOTG_VBUS	USB1_VBUS			
47	PHY	USBOTG_DN	USB1_D_N			
48	PHY	USBOTG_DP	USB1_D_P			
POWER SUPPLY & RESET						
49 50	POW	VIN				3.3V Module power supply input. Input voltage range: 3.3V (-5% min.) to 5V (+10% max.)
51	1V8	#POR		PMIC_RST_B	10K-PU to 1V8	PCA9450C PMIC reset input pin. It is internally pulled up with LDO1 power rail. Once it is asserted low, PMIC performs reset. Leave unconnected, or assert low. Don't drive or pull this pin high externally.
52	3V3	BOOT_MODE	BOOT_MODE0		1K-PD	Boot mode select L: Boot from eMMC / H: Boot from UART/USB
MIPI-CSI						
53	PHY	CSI_D3P_A	MIPI_CSI1_DATA3_P			
54	PHY	CSI_D3N_A	MIPI_CSI1_DATA3_N			
55	PHY	CSI_D2P_A	MIPI_CSI1_DATA2_P			
56	PHY	CSI_D2N_A	MIPI_CSI1_DATA2_N			
57	PHY	CSI_D1P_A	MIPI_CSI1_DATA1_P			
58	PHY	CSI_D1N_A	MIPI_CSI1_DATA1_N			
59	PHY	CSI_D0P_A	MIPI_CSI1_DATA0_P			

PIN	TYPE	QS-STANDARD	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description
			Refer to i.MX8M Plus manuals for details!			
60	PHY	CSI_D0N_A	MIPI_CSI1_DATA0_N			
61	PHY	CSI_CLKP_A	MIPI_CSI1_CLK_P			
62	PHY	CSI_CLKN_A	MIPI_CSI1_CLK_N			
63	PHY	CSI_D3P_B	MIPI_CSI2_DATA3_P			
64	PHY	CSI_D3N_B	MIPI_CSI2_DATA3_N			
65	PHY	CSI_D2P_B	MIPI_CSI2_DATA2_P			
66	PHY	CSI_D2N_B	MIPI_CSI2_DATA2_N			
67	PHY	CSI_D1P_B	MIPI_CSI2_DATA1_P			
68	PHY	CSI_D1N_B	MIPI_CSI2_DATA1_N			
69	PHY	CSI_D0P_B	MIPI_CSI2_DATA0_P			
70	PHY	CSI_D0N_B	MIPI_CSI2_DATA0_N			
71	PHY	CSI_CLKP_B	MIPI_CSI2_CLK_P			
72	PHY	CSI_CLKN_B	MIPI_CSI2_CLK_N			
MISC						
73	3V3	GPIO	GPIO1_IO15	USB2_OTG_OC USDHC3_WP PWM4_OUT CCM_CLKO2	GPIO1[15]	
74	PHY	GPIO	PCIE_REF_PAD_CLK_P			
75	PHY	GPIO	PCIE_REF_PAD_CLK_N			
76	3V3	GPIO	GPIO1_IO06	ENET_QOS_MDC ISP_SHUTTER_TRIG_1 USDHC1_CD_B CCM_EXT_CLK3	GPIO1[06]	
Display Control						
77	3V3	**DISP_EN**	GPIO1_IO08	ENET_QOS_1588_EVENT0_IN PWM1_OUT ISP_PRELIGHT_TRIG_1 ENET_QOS_1588_EVENT0_AUX_IN USDHC2_RESET_B	GPIO1[08]	
78	3V3	**DISP_BL**	GPIO1_IO01	PWM1_OUT ISP_SHUTTER_TRIG_0 CCM_EXT_CLK2	GPIO1[01]	
MIPI-DSI						
79	PHY	DSI_D3P	MIPI_DSI_DATA3_P			
80	PHY	DSI_D3N	MIPI_DSI_DATA3_N			
81	PHY	DSI_D2P	MIPI_DSI_DATA2_P			
82	PHY	DSI_D2N	MIPI_DSI_DATA2_N			
83	PHY	DSI_D1P	MIPI_DSI_DATA1_P			
84	PHY	DSI_D1N	MIPI_DSI_DATA1_N			
85	PHY	DSI_D0P	MIPI_DSI_DATA0_P			
86	PHY	DSI_D0N	MIPI_DSI_DATA0_N			

PIN	TYPE	QS-STANDARD	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description
			Refer to i.MX8M Plus manuals for details!			
87	PHY	DSI_CLKP	MIPI_DSI_CLK_P			
88	PHY	DSI_CLKN	MIPI_DSI_CLK_N			
UART						
89	3V3	UART_RXD_A	UART2_RXD	UART2_RX ECSPI3_MISO GPT1_COMPARE3	GPIO5[24]	A53 Debug
90	3V3	UART_TXD_A	UART2_TXD	UART2_TX ECSPI3_SS0 GPT1_COMPARE2	GPIO5[25]	
91	3V3	UART_RXD_B	UART4_RXD	UART4_RX UART2_CTS_B PCIE_CLKREQ_B GPT1_COMPARE1 I2C6_SCL	GPIO5[28]	M7 Debug
92	3V3	UART_TXD_B	UART4_TXD	UART4_TX UART2_RTS_B GPT1_CAPTURE1 I2C6_SDA	GPIO5[29]	
93	3V3	UART_RXD_C	UART1_RXD	UART1_RX ECSPI3_SCLK	GPIO5[22]	
94	3V3	UART_TXD_C	UART1_TXD	UART1_TX ECSPI3_MOSI	GPIO5[23]	
95	3V3	UART_RTS_C	UART3_TXD	UART3_TX UART1_RTS_B USDHC3_VSELECT GPT1_CLK CAN2_RX	GPIO5[27]	NXP: Request to Send **input** signal
96	3V3	UART_CTS_C	UART3_RXD	UART3_RX UART1_CTS_B USDHC3_RESET_B GPT1_CAPTURE2 CAN2_TX	GPIO5[26]	NXP: Clear to Send **output** signal
2nd SPI						
97	3V3	SPI_NSS_B	ECSPI1_SS0	ECSPI1_SS0 UART3_RTS_B I2C2_SDA SAI7_TX_SYNC	GPIO5[09]	
98	3V3	SPI_MISO_B	ECSPI1_MISO	ECSPI1_MISO UART3_CTS_B I2C2_SCL SAI7_RX_DATA[0]	GPIO5[08]	
99	3V3	SPI_MOSI_B	ECSPI1_MOSI	ECSPI1_MOSI UART3_TX I2C1_SDA SAI7_RX_BCLK	GPIO5[07]	
100	3V3	SPI_SCK_B	ECSPI1_SCLK	ECSPI1_SCLK UART3_RX I2C1_SCL SAI7_RX_SYNC	GPIO5[06]	
USB3						
25A	PHY	USB_TXN	USB2_TXN			
26A	PHY	USB_TXP	USB2_TXP			
50A	PHY	USB_RXN	USB2_RXN			
51A	PHY	USB_RXP	USB2_RXP			
PCIe						
75A	PHY	PCIE_TXN_P	PCIE_TXN_P			
76A	PHY	PCIE_TXN_M	PCIE_TXN_M			
100A	PHY	PCIE_RXN_P	PCIE_RXN_P			
1A	PHY	PCIE_RXN_M	PCIE_RXN_M			

LDO5*) PCA9450 PMIC LDO5 / Default 3V3 / Can be set to 1V8 for low voltage RGMII support

Pins used for manufacturing and debugging – leave unconnected					
PIN		**PIN**		**PIN**	
C1	JTAG_TDI			C3	JTAG_TCK
		B2	JTAG_TDO		
A1	JTAG_BSCAN			A3	JTAG_TMS

JTAG_BSCAN is connected to i.MX8M Plus Pads BOOT_MODE[1:3] and JTAG_MOD, 10K-PD

Onboard peripherals wiring

USED FOR		i.MX8M Plus Pad Name	Alternate functions	GPIO	Description
		Refer to i.MX8M Plus manuals for details!			
eMMC	CMD	NAND_WP_B	USDHC3_CMD	GPIO3[18]	
	CLK	NAND_WE_B	USDHC3_CLK	GPIO3[17]	
	DAT0	NAND_DATA04	USDHC3_DATA0	GPIO3[10]	
	DAT1	NAND_DATA05	USDHC3_DATA1	GPIO3[11]	
	DAT2	NAND_DATA06	USDHC3_DATA2	GPIO3[12]	
	DAT3	NAND_DATA07	USDHC3_DATA3	GPIO3[13]	
	DAT4	NAND_RE_B	USDHC3_DATA4	GPIO3[15]	
	DAT5	NAND_CE2_B	USDHC3_DATA5	GPIO3[3]	
	DAT6	NAND_CE3_B	USDHC3_DATA6	GPIO3[4]	
	DAT7	NAND_CLE	USDHC3_DATA6	GPIO3[5]	
	DS	NAND_CE1_B	USDHC3_STROBE	GPIO3[2]	
PMIC	SDA	I2C1_SDA	I2C1_SDA	GPIO5[15]	10K-PU
	SCL	I2C1_SCL	I2C1_SCL	GPIO5[14]	1K-PU
	IRQ_B	GPIO1_IO03		GPIO1[3]	
	POR_B	POR_B			10K-PU
	PMIC_ON_REQ	PMIC_ON_REQ			
	PMIC_STBY_REQ	PMIC_STBY_REQ			
	WDOG_B	GPIO1_IO02		GPIO1[2]	10K-PU
	CLK_32K_OUT	RTC_XTALI			

Alternate function mappings

PIN FUNC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	21	37	38	39	40	41	42	73	77	78	89	90	91	92	93	94	95	96	97	98	99	100
UART1																RTS_B		CTS_B	RX	TX															RXD	TXD	RTS_B	CTS_B				
UART2																					TX	RX								RXD	TXD	CTS_B	RTS_B								
UART3																																				TXD	RXD	RTS_B	CTS_B	TX	RX
UART4	RTS_B	CTS_B	TX	RX																			RX	TX								RXD	TXD								
SAI1													TX_BCLK	TX_DATA[																											
SAI2															TXD0	RXD0	TXC	TXFS	RXC	RXFS																					
SAI5													MCLK	RXD3	TX_DATA[3]	TX_DATA[0]	TX_DATA[2]	TX_DATA[1]	TX_BCLK	TX_SYNC																					
CAN1											RX	TX					RX																								
CAN2													RX	TX	TX																					RX	TX				
I2C1																																								SDA	SCL
I2C2					SCL	SDA																																SDA	SCL		
I2C3			SDA	SCL				SCL	SDA																																
I2C4	SDA	SCL					SCL			SDA											SCL	SDA																			
I2C5											SDA	SCL	SDA																												
SPI1					MISO	SS0																																SS0	MISO	MOSI	SCLK
SPI2	SS0	MISO	MOSI	SCLK			MISO	SCLK	MOSI	SS0													SCLK	MOSI	MISO	SS0				MISO	SS0			SCLK	MOSI					
SPI3																												OUT	OUT												
PWM1										OUT			OUT														OUT														
PWM2							OUT				OUT																														
PWM3									OUT			OUT																													
PWM4								OUT																		OUT															