QSMP135

QS Family
QFN Style Solder-Down
Computer-on-Modules

- Solder-down version
- 27mm square
- 2.3mm total height
- QFN type lead style
  - 1mm pitch
  - 100 pads
  - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- High speed design compliant
- 3.3V power supply

Key Features

• Processor	STM32MP135C Arm® Cortex®-A7 650MHz
• RAM	256MB DDR3L
• ROM	4GB eMMC
• Grade	Industrial
• Temperature	-25°C to 85°C
• Display support	
Display Interface	24-bit RGB
• Connectivity	

  - Gb Ethernet, USB2.0, eMMC/SD
  - UART, I²C, SPI, PWM, SAI, CAN
  - Two additional pin groups for RS485

Cortex®-A7

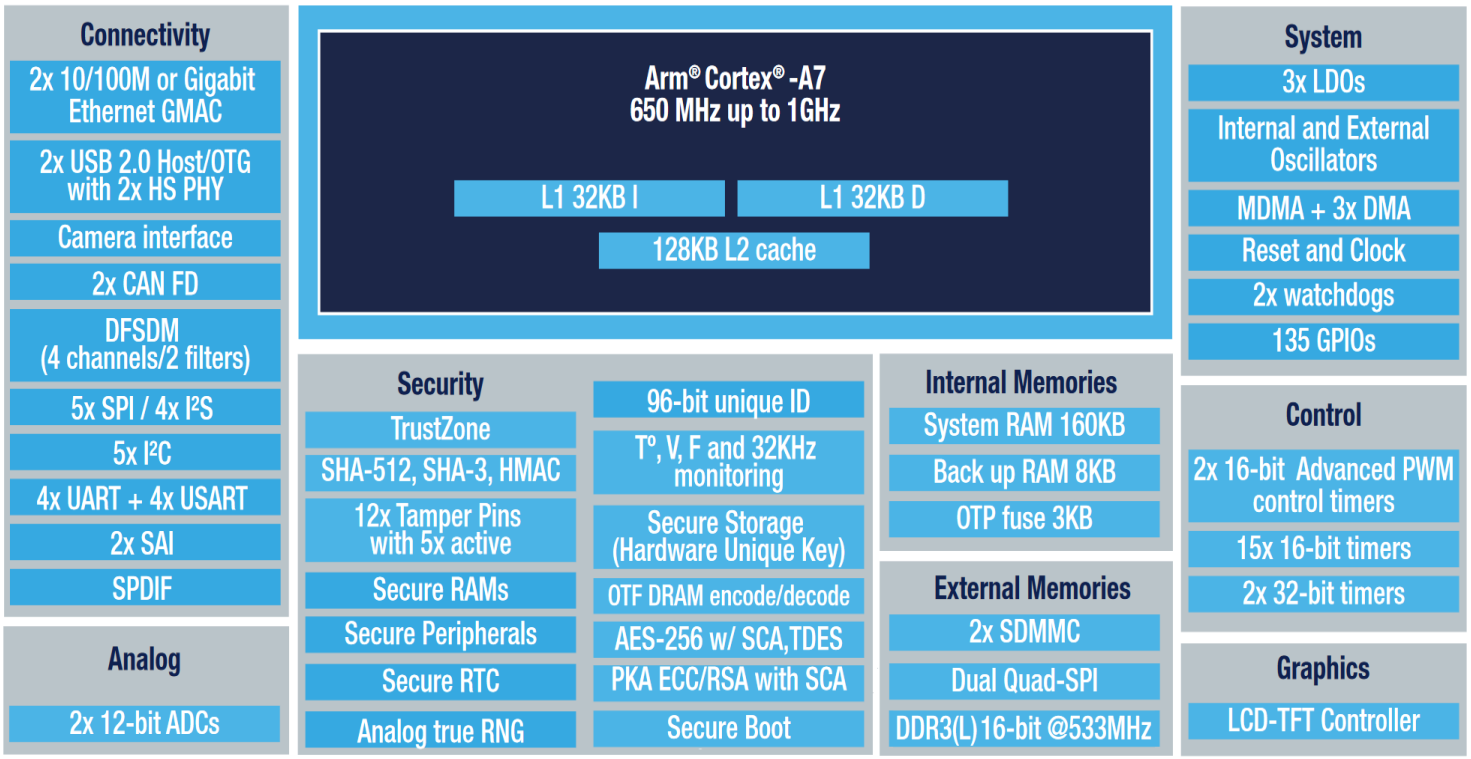
OS Support

- Linux

Authorized Partner

Ka-Ro electronics GmbH - Pascalstr. 22, D-52076 Aachen, Germany - Tel.: +49 2408 1402-0 (FAX -10)
www.karo-electronics.de

STM32MP135 Block Diagram



	QSMP-1351	QSMP-1530C	QSMP-1570
Processor	STM32MP135C	STM32MP157C	
Primary Arm® Core	1x Cortex®-A7 up to 650 MHz	2x Cortex®-A7 up to 650 MHz	
Secondary Arm® Core	-	1x Cortex-M4 up to 200 MHz	
RAM	256 MB	256 MB	512 MB
ROM	4 GB	4 GB	
Display Interface	24-bit RGB	RGB 2-lane MIPI-DSI	
GPU	-	yes	
CAN	yes	yes	
Security	Secure Boot, Cryptography	Secure Boot, Cryptography	
Temperature	-25°C to 85°C	-25°C to 85°C	
Order Code	QSMP/135C/256S/4GF/E85	QSMP/157C/256S/4GF/E85	QSMP/157C/512S/4GF/E85

2024-01-08

Ka-Ro electronics GmbH - Pascalstr. 22, D-52076 Aachen, Germany - Tel.: +49 2408 1402-0 (FAX -10)
www.karo-electronics.de

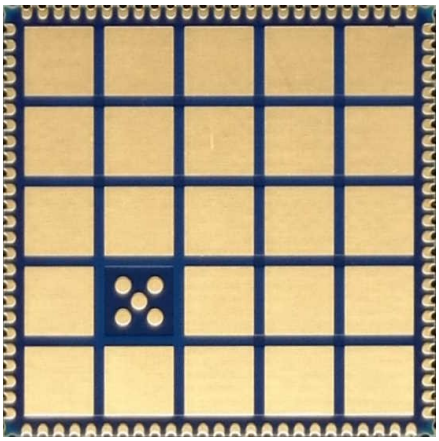
QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He has also provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QSCOM modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.



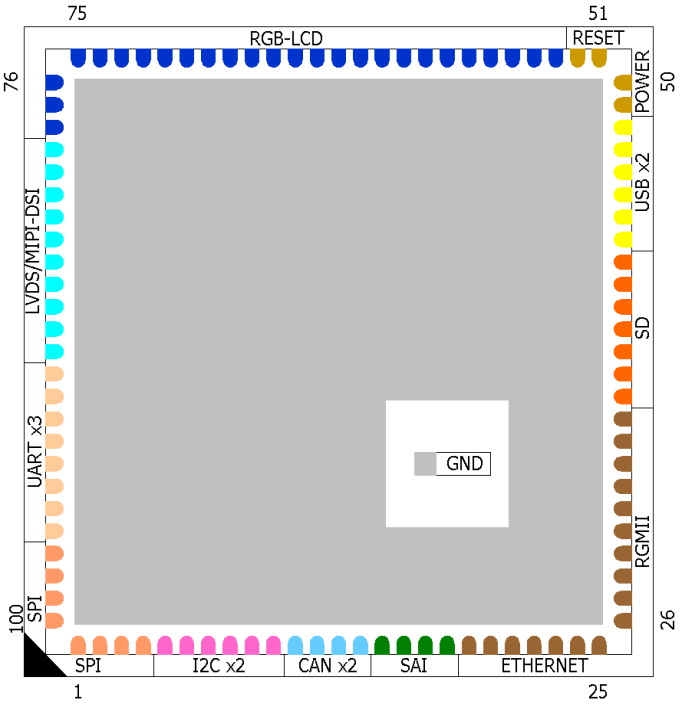
Easy Wiring - Even 2-layer printed circuit boards can be used.

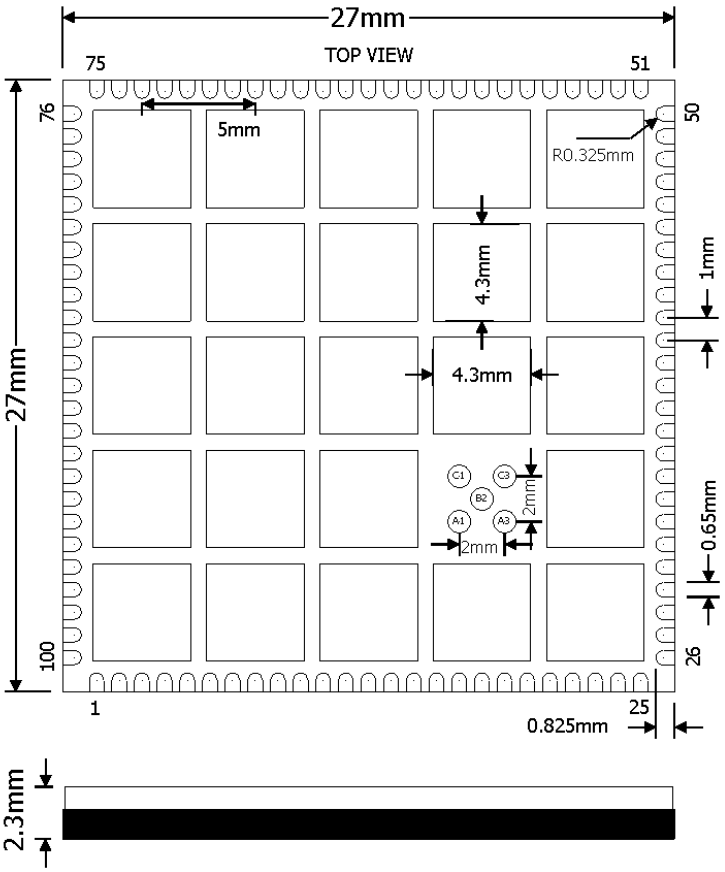
With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing the routing.

Advanced Soldering

Using a large solder pad underneath the component has not only electrical and thermal advantages. This is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight, which could result in short circuits.

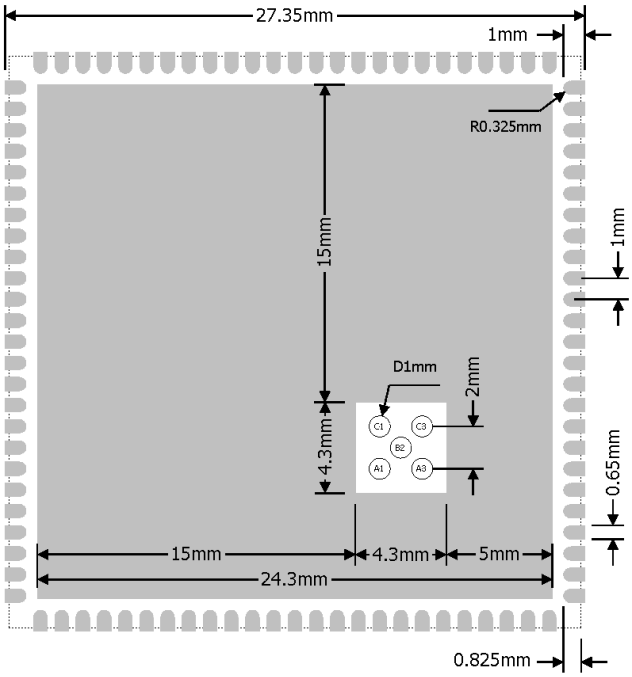
Standard Contact Assignments



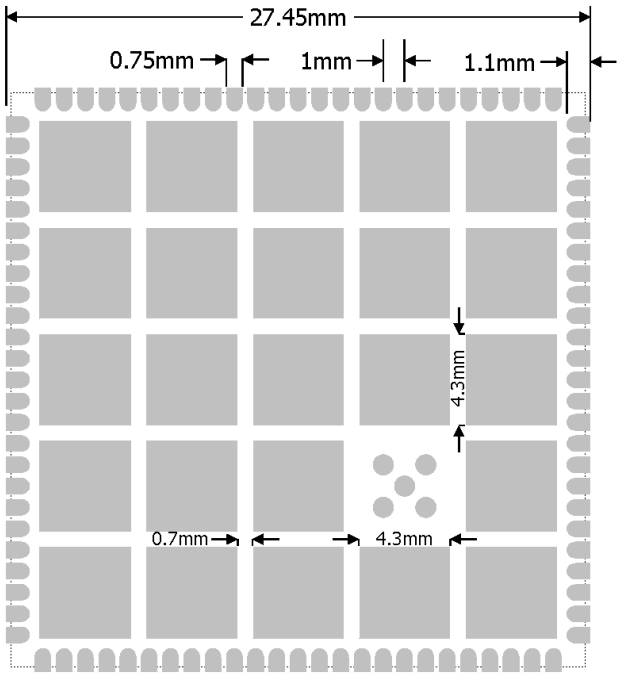


Layout Guidelines

Land pattern

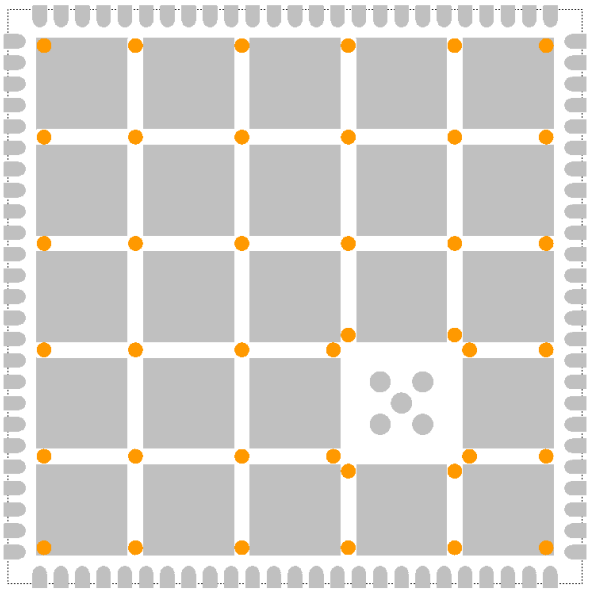


See figure above for the suggested module layout. The five 1mm pads in the square GND pad cutout can be omitted if no JTAG Boundary Scan test is used. The solder mask openings are shown below.



The ground pad solder mask on the bottom side of the QSCOM module is divided into sections for a better reliability of the solder joint and self-alignment of the component.

If the via holes used on the application board have a diameter larger than 0.3 mm, it is recommended to mask the via holes to prevent solder wicking through the via holes. Solders have a habit of filling holes and leaving voids in the thermal pad solder junction, as well as forming solder balls on the other side of the application board which can in some cases be problematic. The 0.7mm wide solder mask stripes can be used to arrange the vias as shown here:

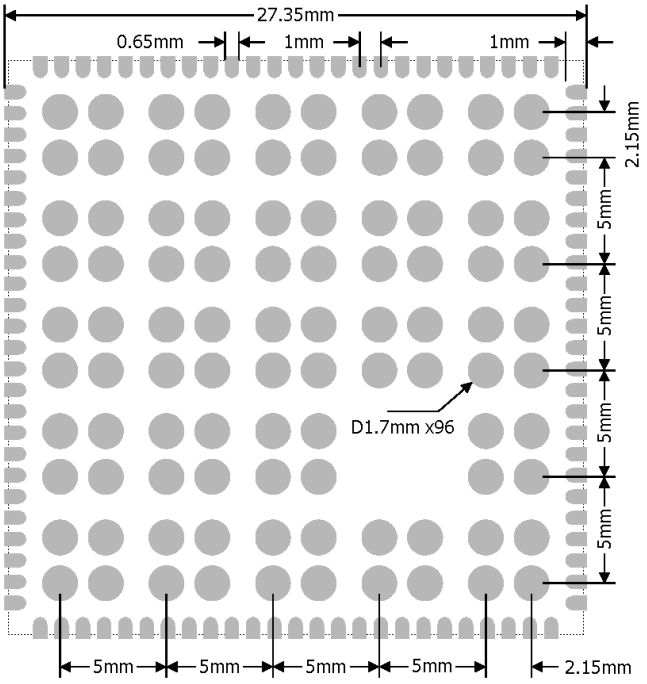


Soldering Recommendations

Ka-Ro QSCOM modules are compatible with industrial standard reflow profile for Pb-free solders. Ka-Ro will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendations should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for reflow profile configurations
- Avoid using more than one flow.
- A 150µm stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, “no clean” solder paste should be used due to low mounted height of the component.

Recommended stencil design

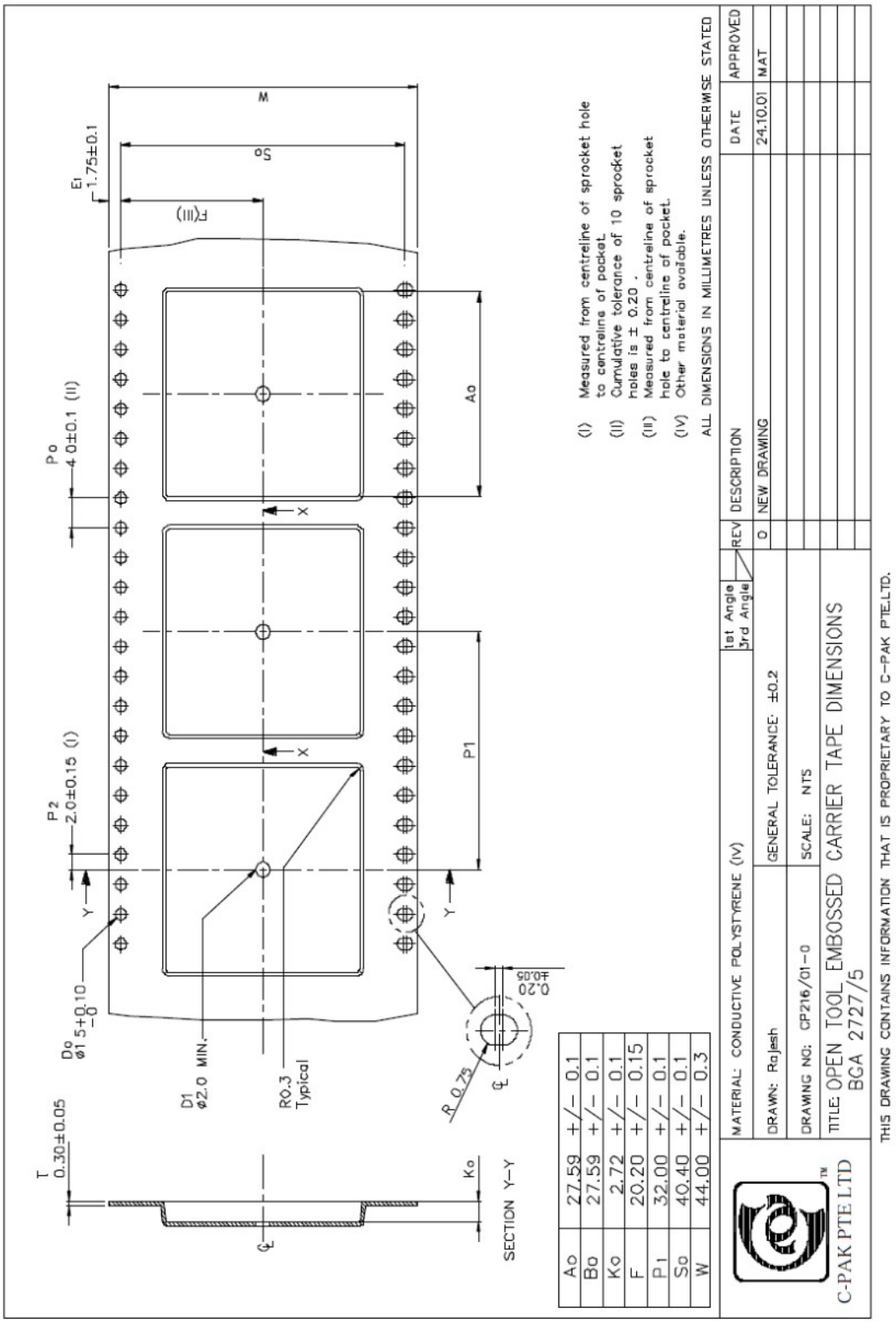


Aperture size of the stencil is 1:1 with the pad size. Four 1.7mm diameter bumps are used for each of the 4.3mm square GND pads sections giving a 50% solder paste padding. The lower component settling with this ensures that the pads at the edge are always soldered even at vertical misalignment by distortion or warping.

Thermal Considerations

The QSCOM module consume more than 1 W of DC power. In any application where high ambient temperatures for more than a few seconds can occur, it is important that a sufficient cooling surface is provided to dissipate the heat. The thermal pad at the bottom of the module must be connected to the application board ground planes by soldering. The application board should provide a number of vias under and around the pad to conduct the produced heat to the board ground planes, and preferably to a copper surface on the other side of the board in order to conduct and spread the heat. The module internal thermal resistance should in most cases be negligible compared to the thermal resistance from the module into air, and common equations for surface area required for cooling can be used to estimate the temperature rise of the module. Only copper planes on the circuit board surfaces with a solid thermal connection to the module ground pad will dissipate heat. For an application with high load the maximum allowed ambient temperature should be reduced due to inherent heating of the module, especially with small fully plastic enclosed applications where heat transfer to ambient air is low due to low thermal conductivity of plastic. The module measured on the evaluation board exhibits a temperature rise of about 20°C above ambient temperature. An insufficiently cooled module will rapidly heat beyond operating range in ambient room temperature.

Packaging


ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED
(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
REV DESCRIPTION DATE APPROVED
0 NEW DRAWING 24.10.01 MAT
MATERIAL: CONDUCTIVE POLYSTYRENE (IV)
1st Angle 3rd Angle
DRAWN: Rajesh
GENERAL TOLERANCE: ±0.2
DRAWING NO: CP216/01-0
SCALE: NTS
TITLE: OPEN TOOL EMBOSSED CARRIER TAPE DIMENSIONS BGA 2727/5
C-PAK PTE LTD
THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO C-PAK PTE.LTD.
SECTION Y-Y
Ao 27.59 +/- 0.1
Bo 27.59 +/- 0.1
Ko 2.72 +/- 0.1
F 20.20 +/- 0.15
P1 32.00 +/- 0.1
So 40.40 +/- 0.1
W 44.00 +/- 0.3

PINOUT (STM32MP1 pads named PA, PB, etc. can be used as GPIO ports)

PIN	QSCOM STANDARD	MP135 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
1st SPI							
1	SPIA_NSS	PA5	- TIM2_CH1 - TIM8_CH1N	SAI1_D1 I2S1_WS/**SPI1_NSS** SAI1_SD_A -	- - ETH1_PPS_OUT ETH2_PPS_OUT	- - - -	
2	SPIA_MISO	PA6	- TIM1_BKIN TIM3_CH1 TIM8_BKIN	SAI2_CK2 I2S1_SDI/**SPI1_MISO** - USART1_CK	- TIM13_CH1 - -	SAI2_SCK_A - - -	
3	SPIA_MOSI	PA3	- TIM2_CH4 TIM5_CH4 LPTIM5_OUT	TIM15_CH2 I2S1_SDO/**SPI1_MOSI** SAI1_FS_B USART2_RX	- - - ETH1_COL	ETH2_COL - - -	
4	SPIA_SCK	PC3	- - SAI1_CK1 DFSDM1_CKOUT	- I2S1_SDI/SPI1_MISO I2S1_CK/**SPI1_SCK** -	UART5_CTS - SAI1_MCLK_A ETH1_TX_CLK	ETH2_TX_CLK - - -	
I2C							
5	I2CA_SCL	PE2	DEBUG_TRACECLK TIM2_CH1 - -	**I2C4_SCL** SPI5_MOSI SAI1_FS_B USART6_DE/USART6_RTS	- SPDIFRX_IN1 ETH2_RXD1 -	FMC_A23 - LTDC_R1 -	
6	I2CA_SDA	PB7	- TIM17_CH1N TIM4_CH2 -	- I2S4_CK **I2C4_SDA** -	- - FMC_NCE2 -	FMC_NL DCMIPP_D13 DCMIPP_PIXCLK -	
7	INTA	**PD12**	- LPTIM1_IN1 TIM4_CH1 -	- I2C1_SCL - -	- - - -	FMC_A17/FMC_ALE DCMIPP_D6 - -	
8	I2CB_SCL	PD1	- - - -	**I2C5_SCL** I2S4_SDO/SPI4_MOSI - -	UART4_TX QUADSPI_BK1_NCS - LTDC_B6	FMC_D3/FMC_DA3 DCMIPP_D13 LTDC_G2 -	
9	I2CB_SDA	PE13	- TIM1_CH3 - -	**I2C5_SDA** I2S4_SDI/SPI4_MISO - -	- - - LTDC_B1	FMC_D10/FMC_DA10 DCMIPP_D4 LTDC_R6 -	
10	INTB	**PE8**	- TIM1_CH1N - DFSDM1_CKIN2	- I2C1_SDA - UART7_TX	- - - -	FMC_D5/FMC_DA5 - - -	
CAN							
11	CANA_RX	PD0	- - SAI1_MCLK_A -	- - SAI1_CK1 -	- **FDCAN1_RX** - -	FMC_D2/FMC_DA2 DCMIPP_D1 - -	
12	CANA_TX	PE10	- TIM1_CH2N - -	- - - UART7_RX	- **FDCAN1_TX** - -	FMC_D7/FMC_DA7 - - -	
13	CANB_RX	PE0	- - - -	- - DCMIPP_D12 -	UART8_RX **FDCAN2_RX** - LTDC_B1	FMC_A11 DCMIPP_D1 LTDC_B5 -	
14	CANB_TX	PB13	DEBUG_TRACECLK TIM1_CH1N - -	LPTIM2_OUT I2S2_WS/SPI2_NSS I2C4_SCL -	SDMMC1_D123DIR **FDCAN2_TX** - UART5_TX	- LTDC_CLK - -	
SAI							
15	SAI_TX	PH11	- SPI5_NSS TIM5_CH2 **SAI2_SD_A**	- I2S2_WS/SPI2_NSS I2C4_SCL USART6_RX	- QUADSPI_BK2_IO0 - ETH2_REF_CLK/RX_CLK	FMC_A12 - LTDC_G6 -	
16	SAI_RX	PG3	- - - TIM8_BKIN2	I2C2_SDA - **SAI2_SD_B** -	- FDCAN2_RX ETH2_GTX_CLK ETH1_MDIO	FMC_A13 DCMIPP_D15 DCMIPP_D12 -	
17	SAI_SCK	PG12	- LPTIM1_IN1 - -	**SAI2_SCK_A** - SAI2_CK2 USART6_DE/USART6_RTS	- - ETH2_PHY_INTN ETH1_PHY_INTN	ETH2_CRS_DV/RX_CTL - - -	

PIN	QSCOM STANDARD	MP135 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
18	SAI_FS	PG1	- LPTIM1_ETR TIM4_ETR **SAI2_FS_A**	I2C2_SMBA I2S2_SDI/SPI2_MISO SAI2_D2 -	- FDCAN2_TX ETH2_TXD2 -	FMC_NBL0 - LTDC_G7 -	
ETHERNET							
19	ENET_RST	**PA4**	- - TIM5_ETR -	SAI1_SCK_B I2S1_WS/SPI1_NSS DFSDM1_CKIN1 -	- - ETH1_PPS_OUT ETH2_PPS_OUT	SAI1_SCK_A - - -	
20	ENET_CK125	PF12	- - - -	- I2S1_WS/SPI1_NSS SAI1_SD_A -	UART4_TX - ETH1_TX_ER **ETH1_CLK125**	- - - -	
21	ENET_INT	PH6	- - TIM12_CH1 -	I2C5_SDA I2S2_CK/SPI2_SCK - -	- - **ETH1_PHY_INTN** ETH1_RX_ER	ETH2_RXD2 QUADSPI_BK1_NCS - -	
22	ENET_MDIO	PA2	- TIM2_CH3 TIM5_CH3 LPTIM4_OUT	TIM15_CH1 - - USART2_TX	- - - **ETH1_MDIO**	- - - -	
23	ENET_MDC	PG2	- RCC_MCO_2 - TIM8_BKIN	- - - -	- - SAI2_MCLK_B **ETH1_MDC**	- DCMIPP_D1 - -	
24	ENET_RXC	PD7	RCC_MCO_1 - - -	I2C2_SCL I2C3_SDA - -	- SPDIFRX_IN0 **ETH1_REF_CLK/RX_CLK** -	FMC_NE1 - - -	
25	ENET_RX_CTL	PA7	- TIM1_CH1N TIM3_CH2 TIM8_CH1N	SAI2_D1 I2S1_CK/SPI1_SCK - USART1_NSS	- TIM14_CH1 - **ETH1_CRS_DV/RX_CTL**	SAI2_SD_A - - -	
26	ENET_RXD0	PC4	- - TIM3_ETR DFSDM1_CKIN2	SAI1_D3 I2S1_MCK - -	UART5_DE/UART5_RTS SPDIFRX_IN2 - **ETH1_RXD0**	SAI2_D3 - - -	
27	ENET_RXD1	PC5	- - - DFSDM1_DATIN2	SAI2_D4 I2S_CKIN SAI1_D4 USART2_CTS	- SPDIFRX_IN3 - **ETH1_RXD1**	- - - -	
28	ENET_RXD2	PB0	DEBUG_DBTRGI TIM1_CH2N TIM3_CH3 TIM8_CH2N	USART1_RX I2S1_MCK SAI2_FS_A USART1_CK	- - SAI2_D2 **ETH1_RXD2**	- - - -	
29	ENET_RXD3	PB1	- TIM1_CH3N TIM3_CH4 TIM8_CH3N	- I2S1_CK/SPI1_SCK DFSDM1_DATIN1 UART4_RX	- - - **ETH1_RXD3**	- - - -	
30	ENET_TX_CTL	PB11	- TIM2_CH4 - LPTIM1_OUT	I2C5_SMBA - - USART3_RX	- - - **ETH1_TX_CTL/TX_EN**	- - - -	
31	ENET_TXC	PC1	- - - DFSDM1_DATIN0	- - SAI1_D3 -	- - ETH1_CRS_DV/RX_DV **ETH1_GTX_CLK**	- - - -	
32	ENET_TXD3	PE5	- - SAI2_SCK_B TIM8_CH3	TIM15_CH1 - - -	UART4_RX - **ETH1_TXD3** -	FMC_NE1 - - -	
33	ENET_TXD2	PC2	- SPI5_NSS - -	- I2S1_WS/SPI1_NSS SAI2_MCLK_A USART1_DE	- - SAI2_CK1 **ETH1_TXD2**	- - - -	
34	ENET_TXD1	PG14	- LPTIM1_ETR - -	- - SAI2_D1 USART6_TX	- - SAI2_SD_A **ETH1_TXD1**	- - - -	
35	ENET_TXD0	PG13	- LPTIM1_OUT - -	- - - USART6_CTS/USART6_NSS	- - - **ETH1_TXD0**	- - - -	
SD							
36	SD_CD	**PB8**	- TIM16_CH1 TIM4_CH3 -	I2C1_SCL I2C3_SCL DFSDM1_DATIN1 -	UART4_RX - SAI1_D1 -	FMC_D13/FMC_DA13 DCMIPP_D6 - -	

PIN	QSCOM STANDARD	MP135 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
37	SD_D1	PC9	DEBUG_TRACED1 - TIM3_CH4 TIM8_CH4	- - - -	UART5_CTS FDCAN1_TX - -	**SDMMC1_D1** - LTDC_B4 -	
38	SD_D0	PC8	DEBUG_TRACED0 - TIM3_CH3 TIM8_CH3	- I2S3_SDI/SPI3_MISO - USART6_CK	- - SAI2_FS_B UART5_DE/UART5_RTS	**SDMMC1_D0** - LTDC_G7 -	
39	SD_CLK	PC12	DEBUG_TRACECLK - - -	- - - -	UART7_TX - SAI2_SD_B -	**SDMMC1_CK** - LTDC_DE -	
40	SD_CMD	PD2	DEBUG_TRACED4 - TIM3_ETR -	I2C1_SMBA I2S3_WS/SPI3_NSS SAI2_D1 USART3_RX	- - - -	**SDMMC1_CMD** - - -	
41	SD_D3	PC11	DEBUG_TRACED3 - - -	I2C1_SDA - I2S3_SDO/SPI3_MOSI -	UART5_RX - SAI2_SCK_B -	**SDMMC1_D3** - - -	
42	SD_D2	PC10	DEBUG_TRACED2 - - -	- I2C1_SCL I2S3_CK/SPI3_SCK USART3_TX	- - SAI2_MCLK_B -	**SDMMC1_D2** - - -	
USB							
43	USBA_VBUS	Not connected					
44	USBA_DN	USB_DM1					
45	USBA_DP	USB_DP1					
46	USBB_VBUS	OTG_VBUS					
47	USBB_DN	USB_DM2					
48	USBB_DP	USB_DP2					
POWER SUPPLY & RESET							
49 50	VIN	3.3V power supply input					
51	NRST_PWREN	This dual function pin is used as reset input and peripheral power supply enable output. NRST_PWREN is directly connected to STM32MP1 NRST and NRST_CORE and enables the DDR memory power supply VDD_DDR. 10nF capacitors on NRST and NRST_CORE protects the device against parasitic resets. The STM32MP1 has permanent internal pull-up resistors to 3.3V. Refer also to STM32MP1 datasheet, chap. 6.3.18 NRST and NRST_CORE pin characteristics.					
52	BOOT_MODE						H: Boot from FLASH L: Boot from UART/USB
DISPLAY							
53	**LCD_DE** CSI_DP2 LVDS1_TX2P	PB5	DEBUG_TRACED4 TIM17_BKIN TIM3_CH2 -	- I2S2_SDI/SPI2_MISO I2C4_SMBA -	SDMMC1_CKIN FDCAN2_RX - UART5_RX	- LTDC_B6 **LTDC_DE** -	
54	**LCD_VSYNC** CSI_DN2 LVDS1_TX2N	PB12	DEBUG_TRACED10 - - -	I2C2_SMBA - DFSDM1_DATIN1 UART7_DE/UART7_RTS	USART3_RX - - UART5_RX	- LTDC_R3 **LTDC_VSYNC** -	
55	**LCD_HSYNC** CSI_DP0 LVDS1_TX0P	PH10	DEBUG_TRACED0 - TIM5_CH1 SAI2_D3	DFSDM1_DATIN2 I2S3_MCK I2S2_SDO/SPI2_MOSI -	- - - -	- **LTDC_HSYNC** LTDC_R2 HDP_HDP0	
56	**LCD_CLK** CSI_DN0 LVDS1_TX0N	PD9	DEBUG_TRACECLK - - DFSDM1_DATIN3	- - - -	- - SDMMC2_CDIR LTDC_B5	FMC_D14/FMC_DA14 **LTDC_CLK** LTDC_B0 -	
57	**LCD_R1** CSI_CKN LVDS1_CLKN	PG7	DEBUG_TRACED8 TIM1_ETR - -	- I2S3_SDI/SPI3_MISO - -	UART7_CTS - SDMMC2_CKIN **LTDC_R1**	- LTDC_R5 LTDC_R2 -	
58	**LCD_R2** CSI_DP1 LVDS1_TX1P	PH8	DEBUG_TRACED9 - TIM5_ETR USART2_RX	I2C3_SDA - - -	- - - LTDC_R6	FMC_A8 DCMIPP_HSYNC **LTDC_R2** HDP_HDP2	
59	**LCD_R3** CSI_DN1 LVDS1_TX1N	PB10	- TIM2_CH3 - LPTIM2_IN1	I2C5_SMBA I2S4_WS/SPI4_NSS I2S2_CK/SPI2_SCK USART3_TX	- - - -	- - **LTDC_R3** -	

PIN	QSCOM STANDARD	MP135 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
60	**LCD_R4** CSI_DP3 LVDS1_TX3P	PD14	- - TIM4_CH3 -	I2C3_SDA - - USART1_RX	- - - -	FMC_D0/FMC_DA0 DCMIPP_D8 **LTDC_R4** -	
61	**LCD_R5** CSI_DN3 LVDS1_TX3N	PE7	- TIM1_ETR - -	LPTIM2_IN1 - - -	UART5_TX - - -	FMC_D4/FMC_DA4 LTDC_B3 **LTDC_R5** -	
62	**LCD_R6** DSI_DP2 LVDS0_TX2P	PA9	- TIM1_CH2 - -	I2C3_SMBA - DFSDM1_DATIN0 USART1_TX	UART4_TX - FMC_NWAIT -	- DCMIPP_D0 **LTDC_R6** -	
63	**LCD_R7** DSI_DN2 LVDS0_TX2N	PD11	- - - LPTIM2_IN2	I2C4_SMBA - - -	SPDIFRX_IN0 - ETH2_CLK125 **LTDC_R7**	FMC_A16/FMC_CLE UART7_RX DCMIPP_D4 -	
64	**LCD_G2**	PH13	DEBUG_TRACED15 - - TIM8_CH1N	I2C5_SCL - I2S3_CK/SPI3_SCK -	UART4_TX - - -	- LTDC_G3 **LTDC_G2** -	
65	**LCD_G3**	PF3	- - - LPTIM2_IN2	I2C5_SDA I2S4_SDI/SPI4_MISO I2S3_WS/SPI3_NSS -	- - - -	FMC_A3 - **LTDC_G3** -	
66	**LCD_G4**	PG5	- TIM17_CH1 - -	- - - -	- - ETH2_MDC **LTDC_G4**	FMC_A15 DCMIPP_VSYNC DCMIPP_D3 -	
67	**LCD_G5**	PG0	- - - -	- - - -	- FDCAN2_TX - -	FMC_A10 DCMIPP_PIXCLK **LTDC_G5** -	
68	**LCD_G6**	PE12	- TIM1_CH3N - -	- I2S4_CK/SPI4_SCK - -	UART8_DE LTDC_VSYNC - LTDC_G4	FMC_D9/FMC_DA9 DCMIPP_D11 **LTDC_G6** HDP_HDP4	
69	**LCD_G7**	PA15	DEBUG_TRACED5 TIM2_CH1 - -	- I2S4_MCK - -	UART4_RX LTDC_R0 - **LTDC_G7**	FMC_A9 DCMIPP_D14 DCMIPP_D5 HDP_HDP5	
70	**LCD_B1**	PG8	- TIM2_CH1 - TIM8_ETR	- SPI5_MISO SAI1_MCLK_B **LTDC_B1**	- SPDIFRX_IN2 - -	FMC_NE2 ETH2_CLK DCMIPP_D6 -	
71	**LCD_B2**	PD10	RTC_REFIN - - -	I2C5_SMBA I2S4_WS/SPI4_NSS - -	- LTDC_G5 - LTDC_B7	FMC_D15/FMC_DA15 DCMIPP_VSYNC **LTDC_B2** -	
72	**LCD_B3**	PF2	DEBUG_TRACED1 - - -	I2C2_SCL - DFSDM1_CKIN1 USART6_CK	- SDMMC2_D0DIR - SDMMC1_D0DIR	FMC_A2 LTDC_G4 **LTDC_B3** -	
73	**LCD_B4**	PH14	- - - DFSDM1_DATIN2	I2C3_SDA - DCMIPP_D8 -	UART4_RX - - **LTDC_B4**	- DCMIPP_D2 DCMIPP_PIXCLK -	
74	**LCD_B5**	PD15	- USART2_RX TIM4_CH4 DFSDM1_DATIN2	- - - -	- - - -	FMC_D1/FMC_DA1 - **LTDC_B5** -	
75	**LCD_B6**	PB6	DEBUG_TRACED6 TIM16_CH1N TIM4_CH1 TIM8_CH1	USART1_TX - SAI1_CK2 **LTDC_B6**	- QUADSPI_BK1_NCS - ETH2_MDIO	FMC_NE3 DCMIPP_D5 LTDC_B7 HDP_HDP6	
76	**LCD_B7**	PE15	- TIM2_CH1 TIM1_BKIN USART2_CTS	- - I2C4_SCL -	- - - -	FMC_D12/FMC_DA12 DCMIPP_D10 **LTDC_B7** HDP_HDP7	
Display Control							
77	**LCD_EN**	**PA10**	- TIM1_CH3 - -	- - - -	- - - -	- - - -	
78	**LCD_BL**	PA0	- **TIM2_CH1** TIM5_CH1 TIM8_ETR	TIM15_BKIN - SAI1_SD_B -	UART5_TX - - ETH1_CRS	ETH2_CRS - - -	
MISC							

PIN	QSCOM STANDARD	MP135 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
79	LCD_R0 CSI_CKP LVDS1_CLKP	PE11	- TIM1_CH2 USART2_CTS -	SAI1_D2 I2S4_SDO/SPI4_MOSI SAI1_FS_A USART6_CK	- **LTDC_R0** ETH2_TX_ER ETH1_TX_ER	FMC_D8/FMC_DA8 DCMIPP_D10 LTDC_R5 -	
80	LCD_G0 DSI_DP3 LVDS0_TX3P	PF5	DEBUG_TRACED12 - - -	DFSDM1_CKIN0 I2C1_SMBA - -	- **LTDC_G0** - -	FMC_A5 DCMIPP_D11 LTDC_R5 -	
81	LCD_G1 DSI_DN3 LVDS0_TX3N	PF1	DEBUG_TRACED7 - - -	I2C2_SDA I2S3_SDO/SPI3_MOSI - -	- - - -	FMC_A1 LTDC_B7 **LTDC_G1** HDP_HDP7	
82	LCD_B0	PD5	- - - -	- - - -	- QUADSPI_BK1_IO0 - -	FMC_NWE **LTDC_B0** LTDC_G4 -	
UART-DE							
83		PF9	- TIM17_CH1N TIM1_CH1 DFSDM1_CKIN3	- - SAI1_D4 UART7_CTS	**UART8_RX** TIM14_CH1 QUADSPI_BK1_IO1 -	FMC_A9 - LTDC_B6 -	
84		PE1	- LPTIM1_IN2 - -	- - - -	**UART8_TX** LTDC_HSYNC - LTDC_R4	FMC_NBL1 DCMIPP_D3 DCMIPP_D12 -	
85		PE14	- TIM1_BKIN - -	SAI1_D4 - - -	**UART8_DE** QUADSPI_BK1_NCS - -	FMC_D11/FMC_DA11 DCMIPP_D7 LTDC_G0 -	
86		PD13	- LPTIM2_ETR TIM4_CH2 TIM8_CH2	SAI1_CK1 - SAI1_MCLK_A **USART1_RX**	- - - -	FMC_A18 - LTDC_G4 -	
87		PC0	- - SAI1_SCK_A -	SAI1_CK2 I2S1_MCK I2S1_SDO/SPI1_MOSI **USART1_TX**	- - - -	- - - -	
88		PA12	- TIM1_ETR SAI2_MCLK_A -	- - - **USART1_DE**	- - - ETH2_CRS_DV/ETH2_RX_CTL/ETH2_RX_DV	FMC_A7 DCMIPP_D1 LTDC_G6 -	
UART							
89	UARTA_RXD	PD8	- - - USART2_TX	- I2S4_WS - USART3_TX	**UART4_RX** - - -	- DCMIPP_D9 DCMIPP_D3 -	
90	UARTA_TXD	PD6	- TIM16_CH1N SAI1_D1 -	- - SAI1_SD_A -	**UART4_TX** - - -	- DCMIPP_D4 DCMIPP_D0 -	
91	UARTB_RXD	PG4	DEBUG_TRACED1 TIM1_BKIN2 - -	DFSDM1_CKIN3 - - -	**USART3_RX** - SDMMC2_D123DIR LTDC_VSYNC	FMC_A14 DCMIPP_D8 DCMIPP_D13 HDP_HDP1	
92	UARTB_TXD	PG11	- - - -	SAI2_D3 I2S2_MCK - **USART3_TX**	UART4_TX - ETH2_TXD1 -	FMC_A24 DCMIPP_D14 LTDC_B2 -	
93	UARTC_RXD	PF4	- - - **USART2_RX**	- - - -	- - - ETH2_RXD0	FMC_A4 DCMIPP_D4 LTDC_B6 -	
94	UARTC_TXD	PF13	- TIM2_CH1 SAI1_MCLK_B -	- - DFSDM1_DATIN3 **USART2_TX**	UART5_RX - - -	- - - -	
95	UARTC_CTS	PD3	- - TIM2_CH1 **USART2_CTS**	DFSDM1_CKOUT I2C1_SDA SAI1_D3 -	- - - -	FMC_CLK DCMIPP_D5 - -	**Input** signal
96	UARTC_RTS	PD4	- - - USART2_DE/**USART2_RTS**	- I2S3_SDI/SPI3_MISO DFSDM1_CKIN0 -	- QUADSPI_CLK - LTDC_R1	FMC_NOE LTDC_R4 LTDC_R6 -	
2nd SPI							

PIN	QSCOM STANDARD	MP135 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
97	SPIB_NSS	PF6	- TIM16_CH1 - -	- **SPI5_NSS** - UART7_RX	- - - ETH2_TX_CTL/ETH2_TX_EN	- LTDC_R7 LTDC_G4 -	
98	SPIB_MISO	PE4	- **SPI5_MISO** SAI1_D2 DFSDM1_DATIN3	TIM15_CH1N I2S_CKIN SAI1_FS_A UART7_DE/UART7_RTS	UART8_TX - FMC_NCE2 -	FMC_A25 DCMIPP_D3 LTDC_G7 -	
99	SPIB_MOSI	PH12	- USART2_TX TIM5_CH3 DFSDM1_CKIN1	I2C3_SCL **SPI5_MOSI** SAI1_SCK_A -	- - SAI1_CK2 ETH1_CRS	FMC_A6 DCMIPP_D3 - -	
100	SPIB_SCK	PG10	- - - -	- **SPI5_SCK** SAI1_SD_B -	- FDCAN1_TX QUADSPI_BK2_IO1 -	FMC_NE3 DCMIPP_D2 - -	

Onboard wiring

Pins used for manufacturing and debugging – leave unconnected					
PIN	(MP1 PAD NAME)	**PIN**	(MP1 PAD NAME)	**PIN**	(MP1 PAD NAME)
C1	**JTAG_TDI** (JTDI)			C3	**JTAG_TCK** (JTCK-SWCLK)
		B2	**JTAG_TDO** (JTDO-TRACESWO)		
A1	**JTAG_TRST_B** (NJTRST)			A3	**JTAG_TMS** (JTMS-SWDIO)

PIN	USED FOR	MP1 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks
Onboard peripherals wiring							
	SERIAL FLASH	PB2	- RTC_OUT2 SAI1_D1 -	- I2S_CKIN SAI1_SD_A -	UART4_RX **QUADSPI_BK1_NCS** - ETH2_MDIO	FMC_A6 - LTDC_B4 -	10K-PU
		PF10	- TIM16_BKIN SAI1_D3 TIM8_BKIN	- SPI5_NSS - USART6_DE/USART6_RTS	UART7_DE/UART7_RTS **QUADSPI_CLK** - -	- DCMIPP_HSYNC LTDC_B5 -	10K-PU
		PF8	- TIM16_CH1N TIM4_CH3 TIM8_CH3	- - SAI1_SCK_B USART6_TX	- TIM13_CH1 **QUADSPI_BK1_IO0** -	- DCMIPP_D15 LTDC_B3 -	10K-PU
		PE9	- TIM1_CH1 - -	- - - -	- **QUADSPI_BK1_IO1** - LTDC_HSYNC	FMC_D6/FMC_DA6 DCMIPP_D7 LTDC_R7 HDP_HDP3	10K-PU
	eMMC	PE3	DEBUG_TRACED11 - SAI2_D4 -	TIM15_BKIN I2S4_SDI/SPI4_MISO - -	- FDCAN1_RX **SDMMC2_CK** -	- LTDC_R4 - -	10K-PU
		PG6	DEBUG_TRACED3 TIM17_BKIN TIM5_CH4 SAI2_D1	USART1_RX - SAI2_SD_A -	- - **SDMMC2_CMD** LTDC_G0	- LTDC_DE LTDC_R7 HDP_HDP3	10K-PU
		PB14	DEBUG_TRACED0 TIM1_CH2N TIM12_CH1 TIM8_CH2N	USART1_TX - - -	- - **SDMMC2_D0** -	- LTDC_R0 LTDC_G5 -	10K-PU
		PB15	RTC_REFIN TIM1_CH3N TIM12_CH2 TIM8_CH3N	SAI2_D2 I2S4_SDO/SPI4_MOSI DFSDM1_CKIN2 UART7_CTS	SDMMC1_CKIN - **SDMMC2_D1** -	SAI2_FS_A LTDC_CLK LTDC_B0 -	
		PB3	DEBUG_TRACED2 TIM2_CH2 - -	SAI2_CK1 I2S4_WS/SPI4_NSS - -	SDMMC1_D123DIR - **SDMMC2_D2** LTDC_R6	SAI2_MCLK_A UART7_RX LTDC_B2 -	
		PB4	DEBUG_TRACED14 TIM16_BKIN TIM3_CH1 -	SAI2_CK2 I2S4_CK/SPI4_SCK - -	- - **SDMMC2_D3** LTDC_G1	SAI2_SCK_A LTDC_B6 LTDC_R0 -	
		PF0	DEBUG_TRACED13 - - DFSDM1_CKOUT	- - - -	- - **SDMMC2_D4** -	FMC_A0 LTDC_R6 LTDC_G0 -	
		PB9	DEBUG_TRACED3 - TIM4_CH4 -	- - I2C4_SDA -	- FDCAN1_TX **SDMMC2_D5** UART5_TX	SDMMC1_CDIR LTDC_DE LTDC_B1 -	
		PC6	DEBUG_TRACED2 - TIM3_CH1 TIM8_CH1	DFSDM1_DATIN0 I2S3_MCK - USART6_TX	- SDMMC2_D0DIR **SDMMC2_D6** LTDC_B1	FMC_A19 LTDC_R6 LTDC_HSYNC HDP_HDP2	
		PC7	DEBUG_TRACED4 - TIM3_CH2 TIM8_CH2	- - I2S2_MCK USART6_RX	- SDMMC2_CDIR **SDMMC2_D7** LTDC_R1	- - LTDC_G6 HDP_HDP4	
	LED	PA13					Low: LED on

Electrical characteristics

Absolute maximum ratings

Parameter	Symbol	Min	Max	Remarks
Power supply	VIN	0V	3.9V	
Input voltage on USB VBUS pins	USBA_VBUS USBB_VBUS	0V	6V	
Input voltage on USB DN/DP pins	USBA_DN/DP USBB_DN/DP	0V	5.5V	
Input voltage on any other pins		0V	3.9V	
Storage temperature range	$T_{STORAGE}$	-40°C	150°C	Version without eMMC
		-40°C	85°C	Version with eMMC

Operating ranges

Parameter	Symbol	Min	Max	Remarks
Power supply	VIN	3.1V	3.6V	
I/O input low level voltage	V_{IL}	-	0.3 x VIN	
I/O input high level voltage	V_{IH}	0.7 x VIN	-	
I/O output voltage	Refer to STM32MP13 datasheet, chap. Output voltage levels.			VDD=VIN=3.3V typ.
Operating temperature range	T_{AMB}	-25°C -40°C	85°C	QSMP /E85 QSMP /I
Processor junction temperature	T_J	-40°C	125°C	

Power supply currents

Parameter	Symbol	VIN	Current	Remarks
At U-Boot prompt	I_{UBOOT}	3.3V	TBDmA	All pins left unconnected
At Linux prompt	I_{LINUX}	3.3V	TBDmA	
Sleep	I_{SLEEP}	3.3V	TBDmA	
Maximum calculated	I_{MAX}	3.3V	700mA	Calculated on max. IDD's @ 80% onboard power supply efficiency.
Power supply rating	I_{SUPP}	3.3V	1A	With margin for sizing the power supply

Alternate UART pin mappings

	RX	TX	RTS/DE	CTS/NSS	CK	Remarks
USART1	28, 60, **86**	62, 75, **87**	33, **88**		2, 28	
USART2	58, 74, **93**	22, 89, **94**, 99	**96**	27, 76, 79, **95**		
USART3	30, 40, 54, **91**	42, 59, 89, **92**				
UART4	29, 32, 36, 69, 73, **89**	8, 20, 62, 64, **90**, 92				
UART5	14, 41, 53, 54, 94	61, 78	26, 38	37		
USART6	15	34	5, 17	35	38, 72, 79	
UART7	12, 63, 97	10, 39	54, 98	57, 83		
UART8	13, **83**	**84**, 98	68, **85**			