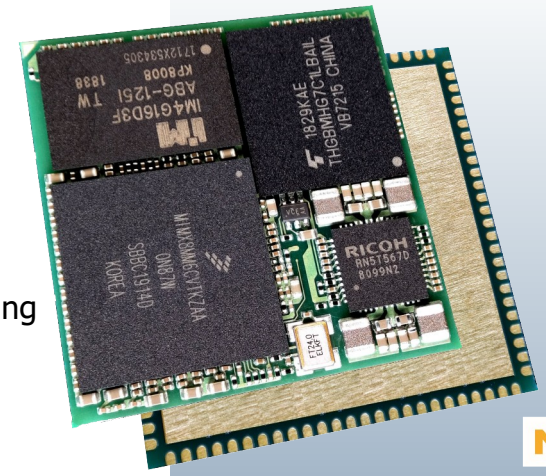
QS8M

QFN Style Solder-Down Computer On Module

- Solder-down version
- 27mm square
- 2.3mm total height
- QFN type lead style
  - 1mm pitch
  - 100 pads
  - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- 3.3V power supply



Key Features

- NXP i.MX 8M Mini — Quad Cortex-A53 up to 1.6GHz, Cortex-M4 up to 400MHz
  NXP i.MX 8M Nano — Dual Cortex-A53 up to 1.4GHz, Cortex-M7 up to 600MHz
- RAM — 512MB/1GB DDR3L
- ROM — 4GB eMMC
- Grade — Industrial
- Temperature — -25°C to 85°C
- Display support

  1x MIPI DSI (4-lane) display interface

  i.MX 8M Mini: GC328 2D GPU, GCNanoUltra 3D GPU, 1080p60 Video de-/encode

  i.MX 8M Nano: GC7000UltraLite 3D GPU

- Connectivity
  - 1x MIPI CSI (4-lane) camera interface
  - 1x Gb Ethernet, 1x/2x USB2.0, 1x eMMC/SD
  - 4x UART, 3x I²C, 2x SPI, 4x PWM, SAI, SPDIF
  - Up to 70x 3.3V General Purpose I/O

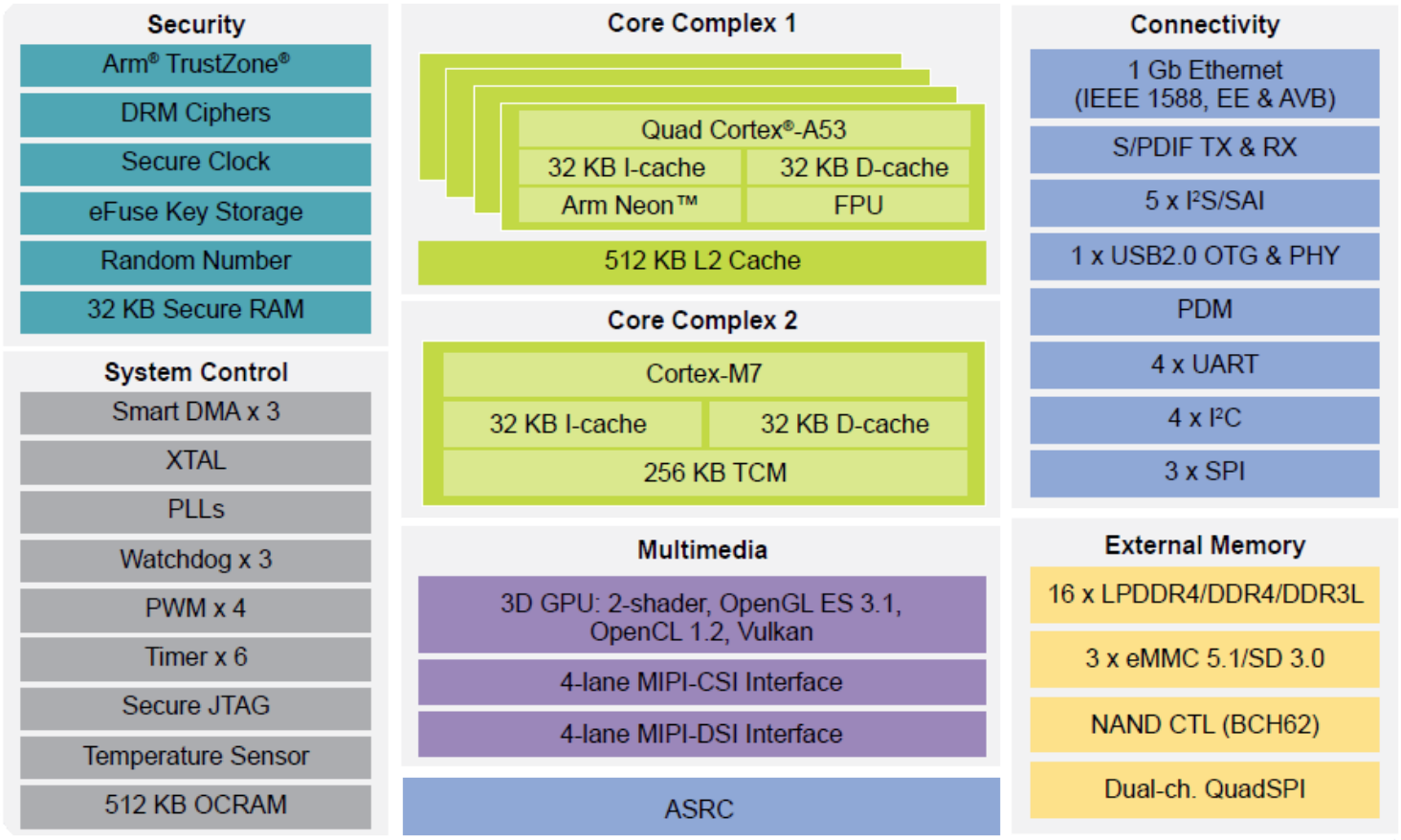
Dual/Quad Cortex®-A53

OS Support

- Linux
- Windows 10 IoT

Ka-Ro electronics GmbH - Pascalstr. 22, D-52076 Aachen, Germany - Tel.: +49 2408 1402-0 (FAX -10)
www.karo-electronics.de

i.MX 8M Nano Block Diagram



QS8M – i.MX 8M Mini and Nano – Differentiated Features and Ordering Information

	QS8M - i.MX 8M Mini	QS8M - i.MX 8M Nano
Primary Arm® Core	4x Cortex®-A53 up to 1.6 GHz	2x Cortex®-A53 up to 1.4 GHz
Secondary Arm® Core	1x Cortex-M4F up to 400 MHz	1x Cortex-M7 up to 600 MHz
RAM	1 GB	512 MB
ROM	4 GB	
GPU	GC328 2D GPU, GCNanoUltra 3D GPU (1x shader, OpenGL ES 2.0)	GC7000UltraLite (2x shader, OpenGL ES 2.0/3.0/3.1 OpenCL 1.2, Vulkan)
Video Decode	1080p60 VP9 Profile 0, 2 (10-bit), HEVC/H.265, AVC/H.264 Baseline, Main, High decoder, VP8	None
Video Encode	1080p60 H.264, VP8	None
Connectivity	2x USB 2.0	1x USB 2.0
Grade / Temperature	Industrial / -25°C to 85°C	
Ordering Information	QS8M/MQ/1GS/4GF/E85	QS8M/ND/512S/4GF/E85

2022-06-15

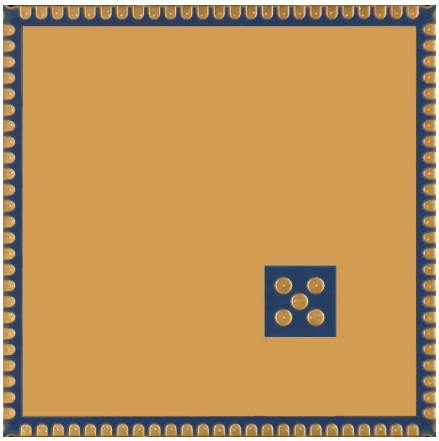
QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He also has to provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QSCOM modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.



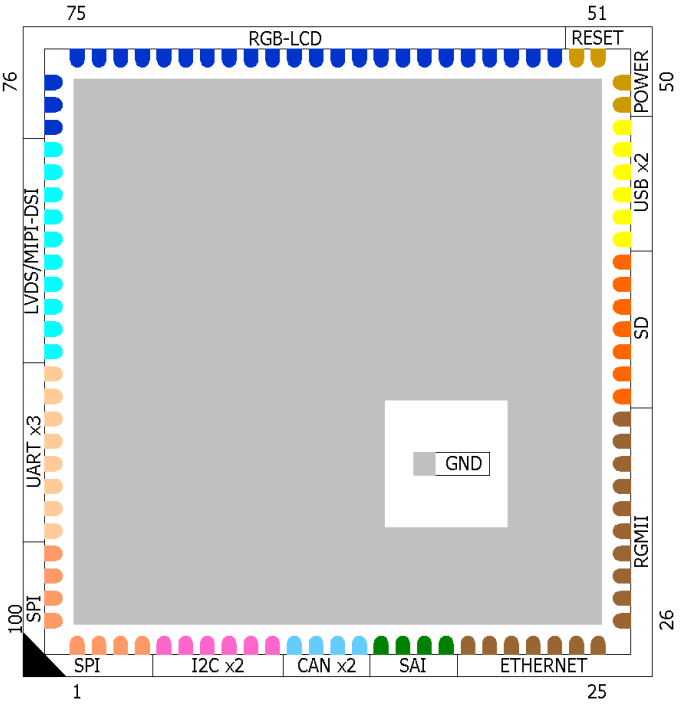
Easy Wiring - Even 2-layer printed circuit boards can be used.

With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing other routes.

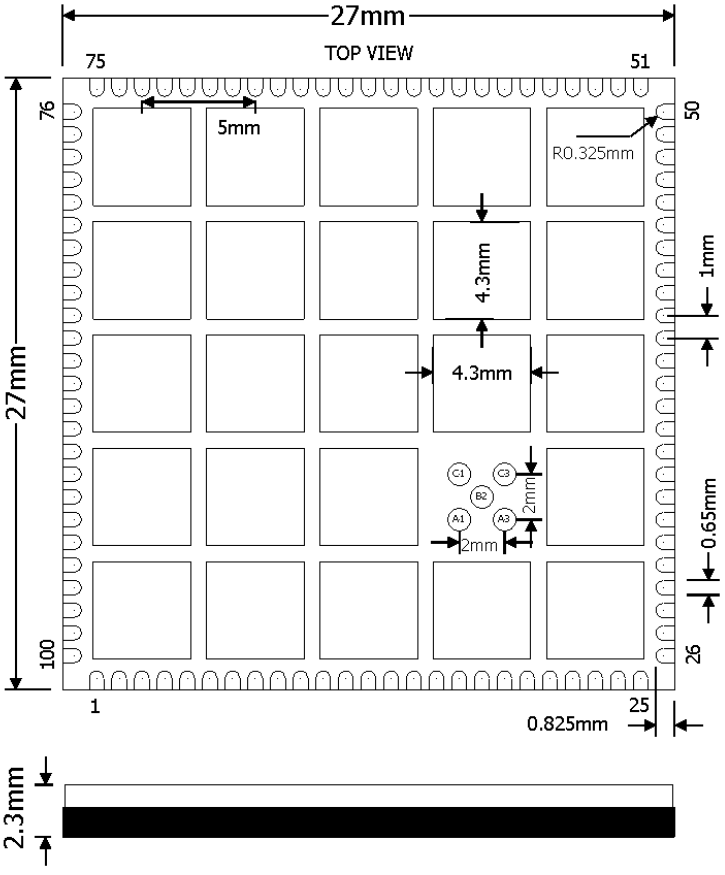
Advanced Soldering

Using a large solder pad underneath the component has not only electrical and thermal advantages. It is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight of the components, which could result in short circuits.

Standard Contact Assignments

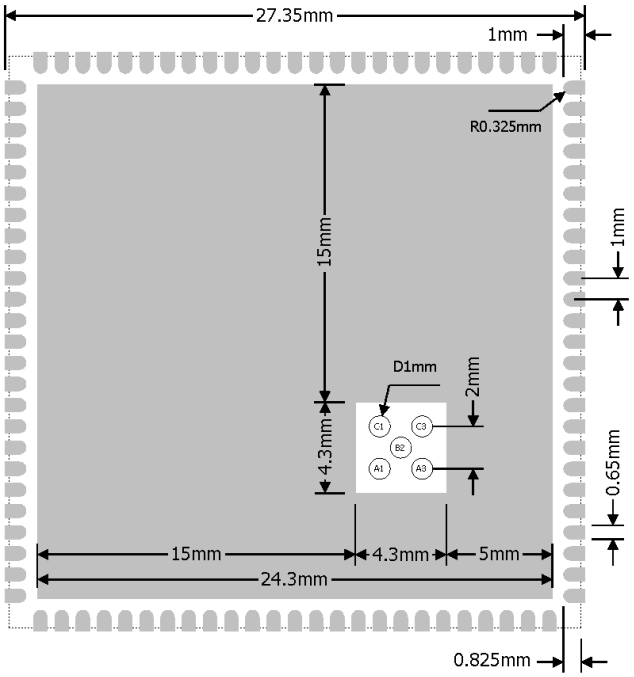


Package Information

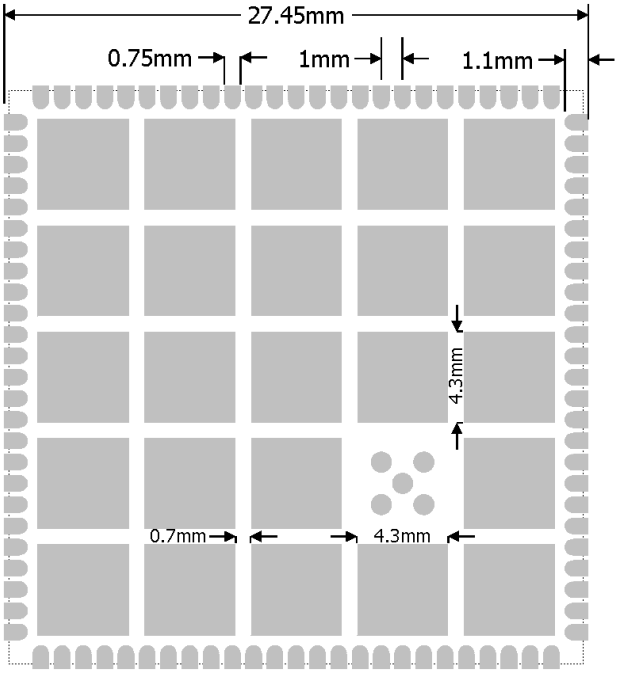


Layout Guidelines

Land pattern

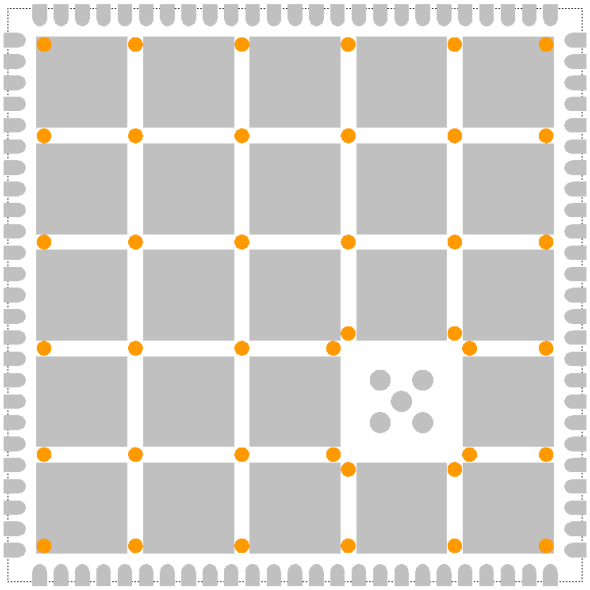


See figure above for the suggested module layout. The five 1mm pads in the square GND pad cutout can be omitted if no JTAG Boundary Scan test is used. The solder mask openings are shown below.



The ground pad solder mask on the bottom side of the QSCOM module is divided into sections for a better reliability of the solder joint and self-alignment of the component.

If the via holes used on the application board have a diameter larger than 0.3 mm, it is recommended to mask the via holes to prevent solder wicking through the via holes. Solders have a habit of filling holes and leaving voids in the thermal pad solder junction, as well as forming solder balls on the other side of the application board which can in some cases be problematic. The 0.7mm wide solder mask stripes can be used to arrange the vias as shown here:

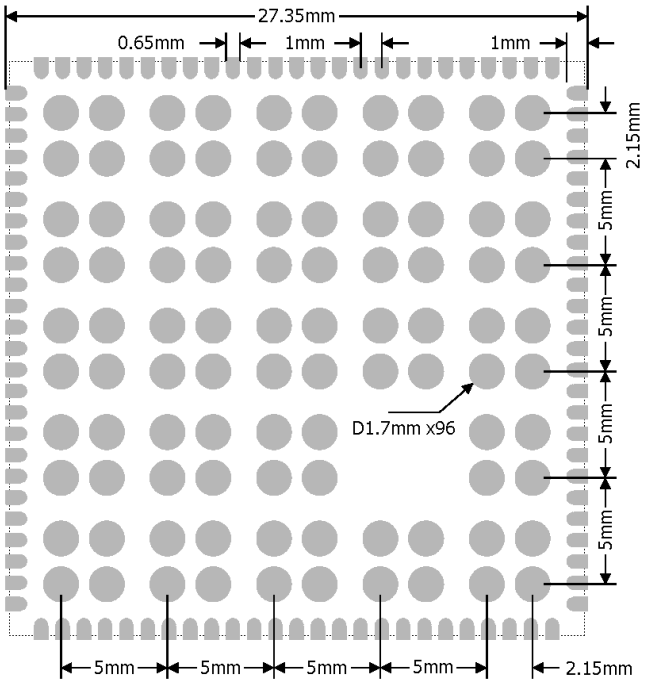


Soldering Recommendations

Ka-Ro QSCOM modules are compatible with industrial standard reflow profile for Pb-free solders. Ka-Ro will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendations should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for reflow profile configurations
- Avoid using more than one flow.
- A 150µm stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, "no clean" solder paste should be used due to low mounted height of the component.

Recommended stencil design

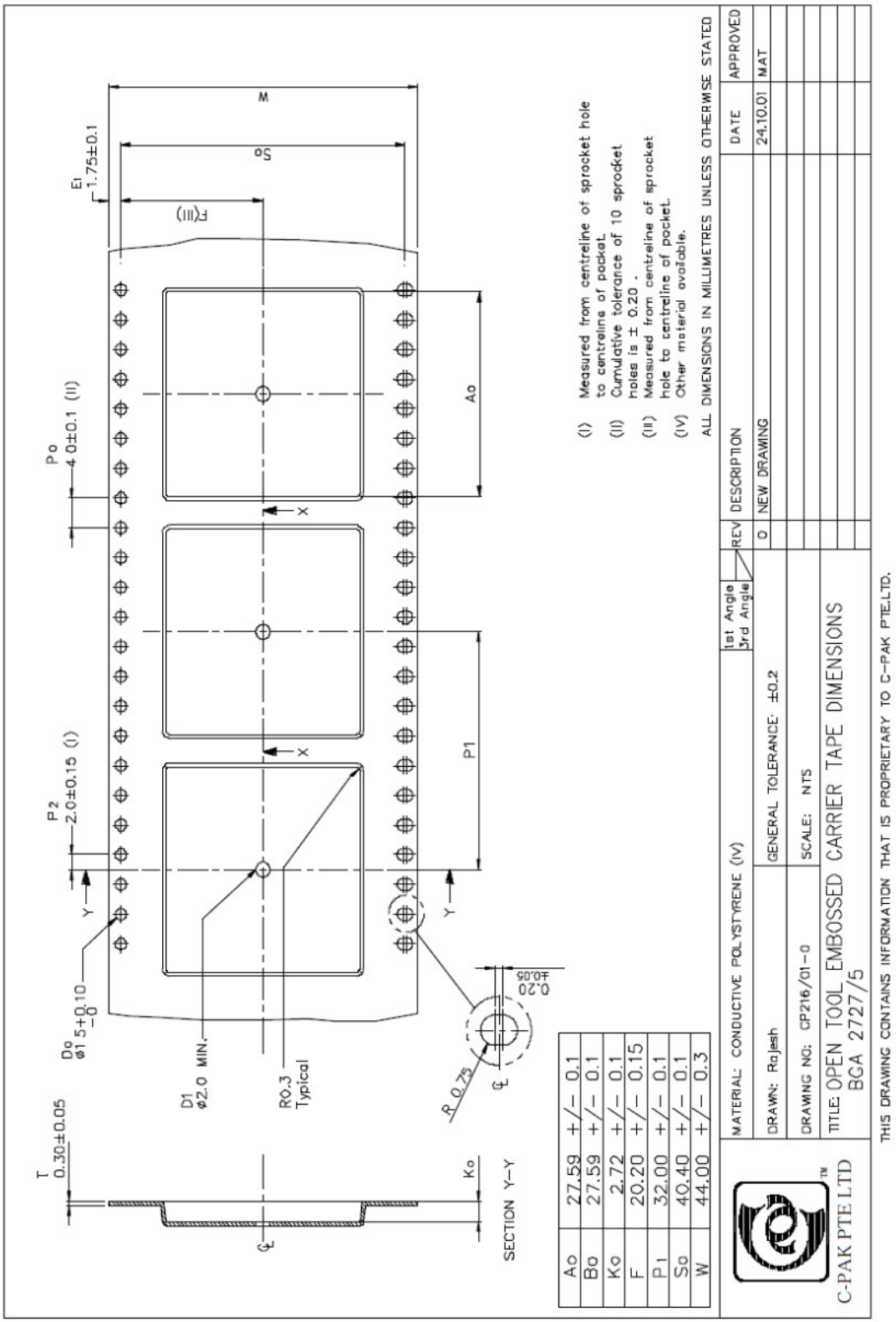


Aperture size of the stencil is 1:1 with the pad size. Four 1.7mm diameter bumps are used for each of the 4.3mm square GND pads sections giving a 50% solder paste padding. The lower component settling with this ensures that the pads at the edge are always soldered even at vertical misalignment by distortion or warping.

Thermal Considerations

The QSCOM module consume more than 1 W of DC power. In any application where high ambient temperatures for more than a few seconds can occur, it is important that a sufficient cooling surface is provided to dissipate the heat. The thermal pad at the bottom of the module must be connected to the application board ground planes by soldering. The application board should provide a number of vias under and around the pad to conduct the produced heat to the board ground planes, and preferably to a copper surface on the other side of the board in order to conduct and spread the heat. The module internal thermal resistance should in most cases be negligible compared to the thermal resistance from the module into air, and common equations for surface area required for cooling can be used to estimate the temperature rise of the module. Only copper planes on the circuit board surfaces with a solid thermal connection to the module ground pad will dissipate heat. For an application with high load the maximum allowed ambient temperature should be reduced due to inherent heating of the module, especially with small fully plastic enclosed applications where heat transfer to ambient air is low due to low thermal conductivity of plastic. The module measured on the evaluation board exhibits a temperature rise of about 20°C above ambient temperature. An insufficiently cooled module will rapidly heat beyond operating range in ambient room temperature.

Packaging


ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED
(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
REV DESCRIPTION DATE APPROVED
0 NEW DRAWING 24.10.01 MAT
MATERIAL: CONDUCTIVE POLYSTYRENE (IV)
1st Angle 3rd Angle
DRAWN: Rajesh
GENERAL TOLERANCE: ±0.2
DRAWING NO: CP216/01-0
SCALE: NTS
TITLE: OPEN TOOL EMBOSSED CARRIER TAPE DIMENSIONS BGA 2727/5
C-PAK PTE LTD
THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO C-PAK PTE.LTD.
Ao 27.59 +/- 0.1
Bo 27.59 +/- 0.1
Ko 2.72 +/- 0.1
F 20.20 +/- 0.15
P1 32.00 +/- 0.1
So 40.40 +/- 0.1
W 44.00 +/- 0.3
SECTION Y-Y

Pinout

PINOUT

PIN	QS STANDARD	i.MX8M Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M manuals for details)
1st SPI					
1	SPIA_NSS	ECSPI2_SS0	UART4_RTS_B	GPIO5[13]	
2	SPIA_MISO	ECSPI2_MISO	UART4_CTS_B	GPIO5[12]	
3	SPIA_MOSI	ECSPI2_MOSI	UART4_TX	GPIO5[11]	
4	SPIA_SCK	ECSPI2_SCLK	UART4_RX	GPIO5[10]	
I2C					
5	I2CA_SCL	I2C2_SCL	ENET1_1588_EVENT1_IN USDHC3_CD_B	GPIO5[16]	
6	I2CA_SDA	I2C2_SDA	ENET1_1588_EVENT1_OUT USDHC3_WP	GPIO5[17]	
7	INTA	I2C4_SCL	PWM2_OUT PCIE1_CLKREQ_B	GPIO5[20]	
8	I2CB_SCL	I2C3_SCL	PWM4_OUT GPT2_CLK	GPIO5[18]	
9	I2CB_SDA	I2C3_SDA	PWM3_OUT GPT3_CLK	GPIO5[19]	
10	INTB	I2C4_SDA	PWM1_OUT	GPIO5[21]	
SPDIF					
11	CANA_RX	SPDIF_TX	SPDIF1_OUT PWM3_OUT	GPIO5[03]	
12	CANA_TX	SPDIF_RX	SPDIF1_IN PWM2_OUT	GPIO5[04]	
13	CANB_RX	SPDIF_EXT_CLK	PWM1_OUT	GPIO5[05]	
14	CANB_TX	SAI2_MCLK	SAI5_MCLK	GPIO4[27]	
SAI					
15	SAI_TX	SAI2_TXD0	SAI2_TX_DATA0 SAI5_TX_DATA3	GPIO4[26]	
16	SAI_RX	SAI2_RXD0	SAI2_RX_DATA0 SAI5_TX_DATA0 UART1_RTS_B	GPIO4[23]	
17	SAI_SCK	SAI2_TXC	SAI2_TX_BCLK SAI5_TX_DATA2	GPIO4[25]	
18	SAI_FS	SAI2_TXFS	SAI2_TX_SYNC SAI5_TX_DATA1 SAI2_TX_DATA1 UART1_CTS_B	GPIO4[24]	
ETHERNET					
19	ENET_RST	SAI2_RXC	SAI2_RX_BCLK SAI5_TX_BCLK UART1_RX	GPIO4[22]	
20	ENET_CK125	GPIO1_IO00	CCM_ENET_PHY_REF_CLK_ROOT XTALOSC_REF_CLK_32K CCM_EXT_CLK1	GPIO1[00]	
21	ENET_INT	GPIO1_IO10	USB1_OTG_ID	GPIO1[10]	
22	ENET_MDIO	ENET_MDIO	ENET1_MDIO IOMUXC_ENET1_MDIO_	GPIO1[17]	
23	ENET_MDC	ENET_MDC	ENET1_MDC	GPIO1[16]	
24	ENET_RXC	ENET_RXC	ENET1_RGMII_RXC ENET1_RX_ER	GPIO1[25]	For RMII—ENET_RXC works as RMII.RX_ERR For RGMII—ENET_RXC works as RGMII.RX_CLK
25	ENET_RX_CTL	ENET_RX_CTL	ENET1_RGMII_RX_CTL	GPIO1[24]	RMII.RX_EN (CRS_DV); RGMII.RC_CTL
26	ENET_RXD0	ENET_RD0	ENET1_RGMII_RD0	GPIO1[26]	RMII and RGMII.RD0
27	ENET_RXD1	ENET_RD1	ENET1_RGMII_RD1	GPIO1[27]	RMII and RGMII.RD1
28	ENET_RXD2	ENET_RD2	ENET1_RGMII_RD2	GPIO1[28]	Only used for RGMII
29	ENET_RXD3	ENET_RD3	ENET1_RGMII_RD3	GPIO1[29]	Only used for RGMII
30	ENET_TX_CTL	ENET_TX_CTL	ENET1_RGMII_TX_CTL	GPIO1[22]	RMII.TX_EN; RGMII.TX_CTL
31	ENET_TXC	ENET_TXC	ENET1_RGMII_TXC ENET1_TX_ER	GPIO1[23]	For RMII—ENET_TXC works as RMII.TX_ERR For RGMII—ENET_TXC works as RGMII.TX_CLK

PIN	QS STANDARD	i.MX8M Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M manuals for details)
32	ENET_TXD3	ENET_TD3	ENET1_RGMII_TD3	GPIO1[18]	Only used for RGMII
33	ENET_TXD2	ENET_TD2	ENET1_RGMII_TD2 INPUT=ENET1_TX_CLK OUTPUT=CCM_ENET_REF_CLK_ROOT	GPIO1[19]	Used as RMII clock and RGMII data, there are two RGMII clock schemes. • MAC generate output 50M reference clock for PHY, and MAC also use this 50M clock. • MAC use external 50M clock.
34	ENET_TXD1	ENET_TD1	ENET1_RGMII_TD1	GPIO1[20]	RMII and RGMII.TD1
35	ENET_TXD0	ENET_TD0	ENET1_RGMII_TD0	GPIO1[21]	RMII and RGMII.TD0
SD					
36	SD_CD	SD2_CD_B	USDHC2_CD_B	GPIO2[12]	
37	SD_D1	SD2_DATA1	USDHC2_DATA1	GPIO2[16]	
38	SD_D0	SD2_DATA0	USDHC2_DATA0	GPIO2[15]	
39	SD_CLK	SD2_CLK	USDHC2_CLK	GPIO2[13]	
40	SD_CMD	SD2_CMD	USDHC2_CMD	GPIO2[14]	
41	SD_D3	SD2_DATA3	USDHC2_DATA3	GPIO2[18]	
42	SD_D2	SD2_DATA2	USDHC2_DATA2	GPIO2[17]	
USB					
43	USBH_VBUS	USB2_VBUS			
	i.MX8M Nano: Not connected				
44	USBH_DN	USB2_DN			
	i.MX8M Nano: Not connected				
45	USBH_DP	USB2_DP			
	i.MX8M Nano: Not connected				
46	USBOTG_VBUS	USB1_VBUS			
47	USBOTG_DN	USB1_DN			
48	USBOTG_DP	USB1_DP			
POWER SUPPLY & RESET					
49 50	VIN				3.3V Module power supply input.
51	#POR		POR_B	10K-PU to 1V8	Power On Reset — 1.8V active low input / open drain output signal. Also connected to PMIC RESETO. Leave unconnected, if not used.
52	BOOT_MODE				Boot mode select L: Boot from eMMC / H: Boot from USB
MIPI-CSI					
53	LCD_DE	MIPI_CSI_DATA3_P			
54	LCD_VSYNC	MIPI_CSI_DATA3_N			
55	LCD_HSYNC	MIPI_CSI_DATA2_P			
56	LCD_CLK	MIPI_CSI_DATA2_N			
57	LCD_R1	MIPI_CSI_DATA1_P			
58	LCD_R2	MIPI_CSI_DATA1_N			
59	LCD_R3	MIPI_CSI_DATA0_P			
60	LCD_R4	MIPI_CSI_DATA0_N			

PIN	QS STANDARD	i.MX8M Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M manuals for details)
61	LCD_R5	MIPI_CSI_CLK_P			
62	LCD_R6	MIPI_CSI_CLK_N			
GPIO					
63	LCD_R7	GPIO1_IO02	WDOG1_WDOG_B WDOG1_WDOG_ANY SJC_DE_B	GPIO1[02]	
64	LCD_G2	GPIO1_IO04	USDHC2_VSELECT SDMA1_EXT_EVENT1	GPIO1[04]	
65	LCD_G3	GPIO1_IO05	M4_NMI CCM_PMIC_READY	GPIO1[05]	
66	LCD_G4	GPIO1_IO06	ENET1_MDC USDHC1_CD_B CCM_EXT_CLK3	GPIO1[06]	
67	LCD_G5	GPIO1_IO07	ENET1_MDIO USDHC1_WP CCM_EXT_CLK4	GPIO1[07]	
68	LCD_G6	GPIO1_IO08	ENET1_1588_EVENT0_IN USDHC2_RESET_B	GPIO1[08]	
69	LCD_G7	GPIO1_IO09	ENET1_1588_EVENT0_OUT USDHC3_RESET_B SDMA2_EXT_EVENT0	GPIO1[09]	
70	LCD_B1	GPIO1_IO11	USB2_OTG_ID USDHC3_VSELECT CCM_PMIC_READY	GPIO1[11]	
71	LCD_B2	GPIO1_IO12	USB1_OTG_PWR SDMA2_EXT_EVENT1	GPIO1[12]	
72	LCD_B3	GPIO1_IO13	USB1_OTG_OC PWM2_OUT	GPIO1[13]	
73	LCD_B4	GPIO1_IO14	USB2_OTG_PWR USDHC3_CD_B PWM3_OUT CCM_CLKO1	GPIO1[14]	
74	LCD_B5	GPIO1_IO15	USB2_OTG_OC USDHC3_WP PWM4_OUT CCM_CLKO2	GPIO1[15]	
75	LCD_B6	SD2_RESET_B	USDHC2_RESET_B SRC_SYSTEM_RESET	GPIO2[19]	
76	LCD_B7	SD2_WP	USDHC2_WP	GPIO2[20]	
Display Control					
77	**DISP_EN**	SAI2_RXFS	SAI2_RX_SYNC SAI5_TX_SYNC SAI5_TX_DATA1 SAI2_RX_DATA1 UART1_TX	GPIO4[21]	
78	**DISP_BL**	GPIO1_IO01	**PWM1_OUT** XTALOSC_REF_CLK_24M CCM_EXT_CLK2	GPIO1[01]	
MIPI-DSI					
79	LCD_R0 **DSI_DP3** LVDS_TX3P	MIPI_DSI_DATA3_P			
80	LCD_G0 **DSI_DN3** LVDS_TX3N	MIPI_DSI_DATA3_N			
81	LCD_G1 **DSI_DP2** LVDS_TX2P	MIPI_DSI_DATA2_P			
82	LCD_B0 **DSI_DN2** LVDS_TX2N	MIPI_DSI_DATA2_N			
83	**DSI_DP1** LVDS_TX1P	MIPI_DSI_DATA1_P			
84	**DSI_DN1** LVDS_TX1N	MIPI_DSI_DATA1_N			
85	**DSI_DP0** LVDS_TX0P	MIPI_DSI_DATA0_P			
86	**DSI_DN0** LVDS_TX0N	MIPI_DSI_DATA0_N			

PIN	QS STANDARD	i.MX8M Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M manuals for details)
87	**DSI_CKP** LVDS_CLKP	MIPI_DSI_CLK_P			
88	**DSI_CKN** LVDS_CLKN	MIPI_DSI_CLK_N			
UART					
89	UARTA_RXD	**UART1_RXD**	UART1_RX ECSPI3_SCLK		
90	UARTA_TXD	**UART1_TXD**	UART1_TX ECSPI3_MOSI		
91	UARTB_RXD	**UART3_RXD**	UART3_RX UART1_CTS_B USDHC3_RESET_B		
92	UARTB_TXD	**UART3_TXD**	UART3_TX UART1_RTS_B USDHC3_VSELECT		
93	UARTC_RXD	**UART2_RXD**	UART2_RX ECSPI3_MISO	GPIO5[24]	
94	UARTC_TXD	**UART2_TXD**	UART2_TX ECSPI3_SS0	GPIO5[25]	
95	UARTC_RTS	UART4_TXD	UART4_TX **UART2_RTS_B**	GPIO5[29]	NXP: Request to Send **input** signal
96	UARTC_CTS	UART4_RXD	UART4_RX **UART2_CTS_B** PCIE1_CLKREQ_B	GPIO5[28]	NXP: Clear to Send **output** signal
2nd SPI					
97	SPIB_NSS	ECSPI1_SS0	UART3_RTS_B	GPIO5[09]	
98	SPIB_MISO	ECSPI1_MISO	UART3_CTS_B	GPIO5[08]	
99	SPIB_MOSI	ECSPI1_MOSI	UART3_TX	GPIO5[07]	
100	SPIB_SCK	ECSPI1_SCLK	UART3_RX	GPIO5[06]	

Pins used for manufacturing and debugging – leave unconnected

PIN		PIN		PIN	
C1	JTAG_TDI			C3	JTAG_TCK
		B2	JTAG_TDO		
A1	JTAG_TRST_B			A3	JTAG_TMS