TX25

Computer On Module

- Processor NXP i.MX257, 400 MHz
- RAM 64 MB SDRAM
- ROM 128MB NAND Flash
- Power supply Single 3.1V to 5.5V
- Size 26mm SO-DIMM
- Temp.-Range -40°C..85°C

454 MHz ARM9

Key Features

- 10/100Mbps Ethernet
- High-Speed USB 2.0 OTG
- Full-Speed USB 2.0 Host
- LCD controller
- Still-picture camera interface
- Several peripheral interfaces:

  UART, SD-CARD, I2C, PWM, 1-wire, Keypad, Digital Audio (AC97/I2S), Configurable serial peripheral interface, 4/5 wire Touchscreen, CAN

OS Support

- Windows Embedded CE
- Linux

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Board highlights:

- Lowest cost 400MHz ARM9
- Industrial temperature range
- Standard TX-DIMM pinout
- as small as possible - only 26mm

The TX25 is a member of a module series, specially designed for NXP Semiconductors' i.MX25 multimedia processors. TX modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TX modules includes a NXP i.MX processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of an LCD screen. The TX25 is specifically targeted at embedded applications where size, high cpu-performance and cost are critical factors.

Computer on module

- NXP i.MX257, 400 MHz
- 64 MByte SDRAM (16bit)
- 128 MByte NAND Flash memory
- DIMM200-module (67,6mm x 26 mm x 3,6mm)
- Operating temperature range -40..85°C

Processor

The i.MX257 processor introduces several key new features such as 3.3V I/O support, three general-purpose 12-bit ADCs, a touch screen controller and integrated 128K SRAM to improve system performance or low-power LCD refresh.

Standard TX-DIMM pinout:

- 4-wire UARTs (x3)
- LCD
- CSI (CMOS Sensor Interface)
- I2C / 1-wire / PWM
- SSI/AC97/I2S (x2)
- 4-wire SD-Card/SDIO
- Keypad 4x4
- CSPI (Configurable serial peripheral interface)

High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- 480 Mbps USB OTG
- 12 Mbps USB Host

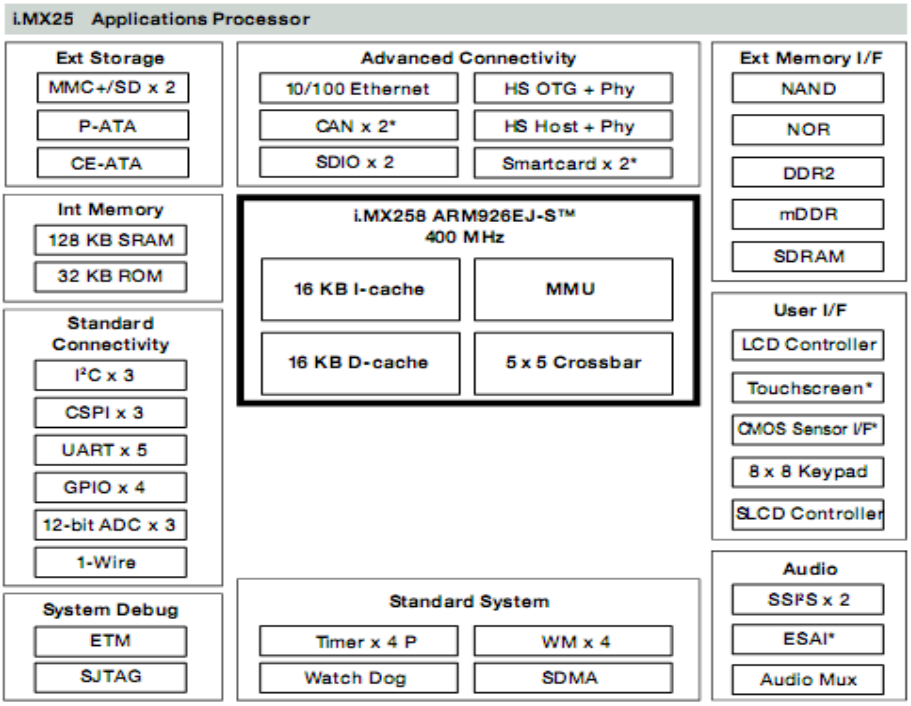
Additional interfaces like CAN, 4/5-wire resistive touch-screen, 2 UARTs and external memory interface are available on TX25 specific pins. Some interfaces are multiplexed with other functions.

Power Supply
The TX25 accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (3.1V to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

Read more in our TX-Guide:

www.karo-electronics.com/TX-Guide



Ordering Information

Order Number	CPU	SDRAM	Flash	Temp.
TX25/400/64S/128F/I	400MHz i.MX257	64MB	128MB	-40°C..85°C

2016-02-03

PINOUT			Marked yellow: Not connected			
PIN	**Type**	**Function**	**i.MX25 Pad Name**	**Alternate functions**	**GPIO**	**Description (refer to I.MX25 manuals for details)**
POWER SUPPLY & RESET						
1-4	power	VIN				Module power supply input (3.0V-5.5V)
5-7, 9-12	power	VOUT				3.3V power supply output **(up to 0.2A)**
8	3V3	BOOTMODE			10K-PU	Boot mode select H: Boot from NAND / L: Boot from UART/USB
13	power		BAT_VDD			DRYICE backup power supply input **(max. 1.55V)**
14	NC					not connected
15	3V3		VSTBY_ACK	HRESET_B SS3 EPITO	GPIO3[18]	"Pulse" indication on finish of internal system reset, by visibility of "hreset_b" signal. After reset, this pin can be used for other purposes.
16	3V3	#POR				Power On Reset - active low input signal. Typically a push button reset. Pull low to force a reset. Leave unconnected or connect to 3V3 if unused. 63.5kΩ pull-up resistor.
17	3V3	RESET_IN_B	RESET_IN_B			Master Reset - external active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset.
18	GND	GND				
Ethernet						
19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LINKLED				Active low LINK ON indication: Active indicates that the link is on.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_ACTLED				Active low ACTIVITY indication: Active indicates that there is Carrier sense (CRS) from the active PMD.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB-HOST						
27	3V3	USBH_VBUSEN	D9	LCDC_LD[22] **USBH2_PWR**	GPIO4[11]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	D8	LCDC_LD[23] **USBH2_OC**	GPIO4[12] 10K-PU	Active low over-current indicator input connected to a GPIO. This signal can be used as an input only. 10kΩ pull-up resistor.
29	analog	USBH_DM	**USBPHY2_DM**			D- pin of the USB cable
30	NC					not connected
31	analog	USBH_DP	**USBPHY2_DP**			D+ pin of the USB cable
32	GND	GND				
USB-OTG						
33	3V3	USBOTG_ID	**USBPHY1_UID**			ID pin of the USB cable. For an A-Device ID is grounded. For a B-Device ID is floated.
34	3V3	USBOTG_VBUSEN	GPIO_A	**USBOTG_PWR** ROW[4] / SCL TXCAN / PWM0 INT_MUX_OUT	GPIO1[0]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	analog	USBOTG_DM	**USBPHY1_DP**			D- pin of the USB cable
36	3V3	#USBOTG_OC	GPIO_B	**USBOTG_OC** ROW[5] / SDA RXCAN / PWMO	GPIO1[1] 10K-PU	Active low over-current indicator input connected to a GPIO. 10kΩ pull-up resistor.
37	analog	USBOTG_DP	**USBPHY1_DP**			D+ pin of the USB cable
38	analog	USBOTG_VBUS	**USBPHY1_VBUS**			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
39	GND	GND	-			
I2C						
40	3V3	I2C_DATA	**I2C1_DAT**	SLCDC_DATA[7]	GPIO1[13]	I2C Data

PIN	Type	Function	i.MX25 Pad Name	Alternate functions	GPIO	Description (refer to I.MX25 manuals for details)
41	3V3	I2C_CLK	**I2C1_CLK**	SLCDC_DATA[6]	GPIO1[12]	I2C Clock
PWM						
42	3V3	PWM	**PWM**	PWMO CMPOUT1 USBH2_OC BT_LPB_FREQ[2]	GPIO1[26] 47K-PU	PWM Output
1-WIRE						
43	3V3	OWDAT	RTCK	**LINE** DAT7 SDMA_DBG_PC_13	GPIO3[14]	1-Wire bus. Requires an external pull-up resistor. The recommended resistor is specified by the generic 1-Wire device used in a given system.
CSPI – Configurable Serial Peripheral Interface						
44	3V3	CSPI_SS0	**CSPI1_SS0**	LCDC_LD[16] PWMO SDMA_DBG_EVT_2 SLCDC_CS TRACE[6]	GPIO1[16]	Slave Select (Selectable polarity) signal
45	3V3	CSPI_SS1	**CSPI1_SS1**	SDA / UART3_RTS SDMA_DBG_EVT_3 SLCDC_RS TRACE[7]	GPIO1[17]	Slave Select (Selectable polarity) signal
46	3V3	CSPI_MOSI	**CSPI1_MOSI**	UART3_RXD_MUX SDMA_DBG_EVT_0 SLCDC_DATA[12] TRACE[4]	GPIO1[14]	Master Out/Slave In signal
47	3V3	CSPI_MISO	**CSPI1_MISO**	UART3_TXD_MUX SDMA_DBG_EVT_1 SLCDC_DATA[13] TRACE[5]	GPIO1[15]	Master In/Slave Out signal
48	3V3	CSPI_SCLK	**CSPI1_SCLK**	UART3_CTS SDMA_DBG_EVT_4 SLCDC_DATA[14] TRACE[8]	GPIO1[18]	Serial Clock signal
49	3V3	CSPI_RDY	**CSPI1_RDY**	SDMA_DBG_EVT_5 SLCDC_DATA[15] TRACE[9]	GPIO2[22]	Serial Data Ready signal
50	GND	GND				
SD – Secure Digital Interface 1						
51	3V3	SD1_CD	BCLK	EIM_BCLK	**GPIO4[4]**	SD Card Detect – connected to a GPIO
52	3V3	SD1_D[0]	**SD1_DATA0**	SCLK / TDATA[2] AUD7_TXFS SDMA_DBG_STAT_1 SLCDC_DATA[2] TRACE[12]	GPIO2[25]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	3V3	SD1_D[1]	**SD1_DATA1**	RDY / TDATA[3] AUD7_RXD SDMA_DBG_STAT_2 SLCDC_DATA[3] TRACE[13]	GPIO2[26]	
54	3V3	SD1_D[2]	**SD1_DATA2**	SS0 / RX_CLK AUD7_RXC SDMA_DBG_STAT_3 SLCDC_DATA[4] TRACE[14]	GPIO2[27]	
55	3V3	SD1_D[3]	**SD1_DATA3**	SS1 / CRS AUD7_RXFS SLCDC_DATA[5] TRACE[15]	GPIO2[28]	
56	3V3	SD1_CMD	**SD1_CMD**	MOSI / RDATA[2] SDMA_DBG_EVT_SEL SLCDC_DATA[0] TRACE[10]	GPIO2[23]	SD Command bidirectional signal
57	3V3	SD1_CLK	**SD1_CLK**	MISO / RDATA[3] SDMA_DBG_STAT_0 SLCDC_DATA[1] TRACE[11]	GPIO2[24]	SD Output Clock.
58	GND	GND				
1st UART						
59	3V3	UART1_TXD	**UART1_TXD**	UART2_DSR LCDC_SPL SLCDC_DATA[9]	GPIO4[23]	Transmit Data output signal

PIN	Type	Function	i.MX25 Pad Name	Alternate functions	GPIO	Description (refer to I.MX25 manuals for details)
60	3V3	UART1_RXD	**UART1_RXD**	UART2_DTR LCDC_CLS SLCDC_DATA[8]	GPIO4[22]	Receive Data input signal
61	3V3	UART1_RTS	**UART1_RTS**	CSI_D[0] / CAPIN1 DCD_2 / LCDC_PS SLCDC_DATA[10]	GPIO4[24]	Request to Send input signal
62	3V3	UART1_CTS	**UART1_CTS**	CSI_D[1] / CMPOUT1 RI_2 / LCDC_REV SLCDC_DATA[11]	GPIO4[25]	Clear to Send output signal
2nd UART						
63	3V3	UART2_TXD	**UART2_TXD**	UART2_TXD_MUX DAT6 / TX_ERR EXTDMA_0	GPIO4[27]	Transmit Data output signal
64	3V3	UART2_RXD	**UART2_RXD**	UART2_RXD_MUX DAT7	GPIO4[26]	Receive Data input signal
65	3V3	UART2_RTS	**UART2_RTS**	DAT5 / COL / CAPIN1 EPITO / SS3 / EXTDMA_1	GPIO4[28]	Request to Send input signal
66	3V3	UART2_CTS	**UART2_CTS**	DAT4 / RX_ERR CMPOUT1 / SS3 EXTDMA_2	GPIO4[29]	Clear to Send output signal
3rd UART						
67	3V3	UART5_TXD	ECB	EIM_ECB **UART5_TXD_MUX** SCLK	GPIO3[23]	Transmit Data output signal
68	3V3	UART5_RXD	LBA	EIM_LBA **UART5_RXD_MUX** RDY	GPIO3[24]	Receive Data input signal
69	3V3	UART5_RTS	CS5	EIM_CS5 NANDF_CE2 DTACK_B / **RTS_5** AUD4_RXFS MISO / TRCLK	GPIO3[21]	Request to Send input signal
70	3V3	UART5_CTS	CS4	EIM_CS4 NANDF_CE1 **CTS_5** / AUD4_RXC MOSI / TRSYNC	GPIO3[20]	Clear to Send output signal
71	GND	GND				
KEYPAD						
72	3V3	KP_COL[0]	**KPP_COL0**	UART4_RXD_MUX AUD5_TXD SDMA_DBG_PC_4	GPIO3[1]	Keypad Column selection signals.
73	3V3	KP_COL[1]	**KPP_COL1**	UART4_TXD_MUX AUD5_RXD SDMA_DBG_PC_5	GPIO3[2]	
74	3V3	KP_COL[2]	**KPP_COL2**	RTS_4 / AUD5_TXC SDMA_DBG_PC_6 M3IF_CHOSEN_ MASTER_1	GPIO3[3]	
75	3V3	KP_COL[3]	**KPP_COL3**	CTS_4 / AUD5_TXFS SDMA_DBG_PC_7 M3IF_CHOSEN_ MASTER_2	GPIO3[4]	
76	3V3	TXCAN	GPIO_C	PWMO / SCL CAPIN1 / SS2 TXCAN	GPIO1[2]	Module specific function
77	3V3	KP_ROW[0]	**KPP_ROW0**	UART3_RXD / DTR_1 SDMA_DBG_PC_0	GPIO2[29]	Keypad Row selection signals.
78	3V3	KP_ROW[1]	**KPP_ROW1**	UART3_TXD / DSR_1 SDMA_DBG_PC_1	GPIO2[30]	
79	3V3	KP_ROW[2]	**KPP_ROW2**	RTS_3 / AUD5_RXC CSI_D[0] / DCD_1 SDMA_DBG_PC_2	GPIO2[31]	
80	3V3	KP_ROW[3]	**KPP_ROW3**	CTS_3 / AUD5_RXFS CSI_D[1] / RI_1 SDMA_DBG_PC_3	GPIO3[0]	
81	3V3	RXCAN	GPIO_D	WDOG_B / SDA COL[5] / CMPOUT1 RXCAN / SS2	GPIO1[3]	Module specific function
82	GND	GND				
SSI 1 - Serial Audio Port 1 (Configurable to I2S Protocol and AC97)						
83	3V3	SSI1_INT	EXT_ARMCLK		**GPIO3 [15]**	GPIO
84	3V3	SSI1_RXD	EB1	EIM_EB1_B **AUD4_RXD** / SS1	GPIO2[13]	Receive serial data

PIN	Type	Function	i.MX25 Pad Name	Alternate functions	GPIO	Description (refer to I.MX25 manuals for details)
85	3V3	SSI1_TXD	EB0	EIM_EB0_B **AUD4_TXD** / SS0	GPIO2[12]	Transmit serial data
86	3V3	SSI1_CLK	OE	EIM_OE **AUD4_TXC**	GPIO2[14]	Serial clock
87	3V3	SSI1_FS	RW	EIM_RW **AUD4_TXFS**	GPIO3[25]	Frame Sync
88	GND	GND				
SSI 2 - Serial Audio Port 2 (Configurable to I2S Protocol and AC97)						
89	3V3	SSI2_INT	UPLL_BYPCLK		**GPIO3 [16]**	GPIO
90	3V3	SSI2_RXD	POWER_FAIL	POWER_FAIL_INT **AUD7_RXD** / CTS_4	GPIO3[19]	Receive serial data
91	3V3	SSI2_TXD	GPIO_E	SCL / LCDC_LD[16] **AUD7_TXD** UART4_RXD_MUX CTI_TRIG_IN0_6	GPIO1[4]	Transmit serial data
92	3V3	SSI2_CLK	GPIO_F	LCDC_LD[17] EPITO / **AUD7_TXC** UART4_TXD_MUX CTI_TRIG_OUT0_6	GPIO1[5]	Serial clock
93	3V3	SSI2_FS	VSTBY_REQ	**AUD7_TXFS** UART4_RTS	GPIO3[17]	Frame Sync
94	GND	GND				
Secure Digital Interface 2						
95	NC					not connected
96	NC					not connected
97	NC					not connected
98	NC					not connected
99	NC					not connected
100	NC					not connected
101	NC					not connected
102	GND	GND				
CMOS Sensor Interface						
103	3V3	CSI_D0	**CSI_D2**	UART5_RXD / DAT4 SCKR / CLK0 / MOSI USBOTG_DATA[0]	GPIO1[27]	Sensor port data
104	3V3	CSI_D1	**CSI_D3**	UART5_TXD / DAT5 FSR / RST0 / MISO USBOTG_DATA[1]	GPIO1[28]	Sensor port data
105	3V3	CSI_D2	**CSI_D4**	RTS_5 / DAT6 / HCKR VEN0 / SCLK USBOTG_DATA[2]	GPIO1[29]	Sensor port data
106	3V3	CSI_D3	**CSI_D5**	CTS_5 / DAT7 / SCKT TX0 / RDY USBOTG_DATA[3]	GPIO1[30]	Sensor port data
107	3V3	CSI_D4	**CSI_D6**	ROW[6] / CMD / FST PD0 / SS0 USBOTG_DATA[4]	GPIO1[31]	Sensor port data
108	3V3	CSI_D5	**CSI_D7**	ROW[7] / CLK / HCKT RX0 / SS1 USBOTG_DATA[5]	GPIO1[6]	Sensor port data
109	3V3	CSI_D6	**CSI_D8**	COL[6] / AUD6_RXC TX5_RX0 / CLK0/ SS2 USBOTG_DATA[6]	GPIO1[7]	Sensor port data
110	3V3	CSI_D7	**CSI_D9**	COL[7] / AUD6_RXFS TX4_RX1 / RST0/ SS3 USBOTG_DATA[7]	GPIO4[21]	Sensor port data
111	GND	GND				
112	3V3	CSI_HSYNC	**CSI_HSYNC**	AUD6_TXC / DAT2 TX1 / PD0 BT_RES[2] USBOTG_NXT	GPIO1[10]	Sensor port horizontal sync
113	3V3	CSI_VSYNC	**CSI_VSYNC**	AUD6_RXD / DAT1 TX2_RX3 / TX0 USBOTG_STP BT_RES[1]	GPIO1[9]	Sensor port vertical sync

PIN	Type	Function	i.MX25 Pad Name	Alternate functions	GPIO	Description (refer to I.MX25 manuals for details)
114	3V3	CSI_PIXCLK	**CSI_PIXCLK**	AUD6_TXFS DAT3 / TX0 / RX0 USBOTG_CLK BT_RES[3]	GPIO1[11]	Sensor port data latch clock
115	3V3	CSI_MCLK	**CSI_MCLK**	AUD6_TXD / DAT0 TX3_RX2 / VEN0 USBOTG_DIR BT_RES[0]	GPIO1[8]	Sensor port master clock
116	GND	GND				
LCD Controller and Smart LCD Controller						
117	3V3	GPIO	CLKO		GPIO2[21]	Clock out pin from CRM, clock source is controlable and can also be used for debug.
118	3V3	CONTRAST	CONTRAST	CAPIN1 / SS1 / DA_2 PWMO / CRS USBH2_PWR WDOG_B		
119	3V3	LD0	**LD0**	SLCDC_DATA[0] CSI_D[0] / DATA[0] CLK1 / USBH2_CLK BT_MEM_CTRL[0]	GPIO2[15] 47K-PU	LCD Data Bus
120	3V3	LD1	**LD1**	SLCDC_DATA[1] CSI_D[1] / DATA[1] RST1 / USBH2_DIR BT_MEM_CTRL[1]	GPIO2[16] 10K-PD	LCD Data Bus
121	3V3	LD2	**LD2**	SLCDC_DATA[2] CSI_D[15] / DATA[2] VEN1 / USBH2_STP BT_MEM_TYPE[0]	GPIO2[17] 10K-PD	LCD Data Bus
122	3V3	LD3	**LD3**	SLCDC_DATA[3] CSI_D[14] / DATA[3] TX1 / USBH2_NXT BT_MEM_TYPE[1]	GPIO2[18] 10K-PD	LCD Data Bus
123	3V3	LD4	**LD4**	SLCDC_DATA[4] CSI_D[13] / DATA[4] PD1/ USBH2_DATA[0] BT_PAGE_SIZE[0]	GPIO2[19] 47K-PU	LCD Data Bus
124	3V3	LD5	**LD5**	SLCDC_DATA[5] CSI_D[12] / DATA[5] RX1/ USBH2_DATA[1] BT_PAGE_SIZE[1]	GPIO1[19] 10K-PD	LCD Data Bus
125	3V3	GPIO	A13	EIM_DA_H[13] LCDC_CLS	GPIO4[1]	
126	3V3	GPIO	A15	EIM_DA_H2[15] RST1 / LCDC_PS	GPIO2[1]	
127	3V3	LD6	**LD6**	SLCDC_DATA[6] CSI_D[11] / DATA[6] CLK1 USBH2_DATA[2] BT_BUS_WIDTH[0]	GPIO1[20] 10K-PD	LCD Data Bus
128	3V3	LD7	**LD7**	SLCDC_DATA[7] CSI_D[10] / DATA[7] RST1 USBH2_DATA[3] BT_BUS_WIDTH[1]	GPIO1[21] 10K-PD	LCD Data Bus
129	GND	GND				
130	3V3	LD8	**LD8**	SLCDC_DATA[8] UART4_RXD/DATA[8] AUD3_TXD / TX_ERR CMD BT_USB_SRC[0]	10K-PD	LCD Data Bus
131	3V3	LD9	**LD9**	SLCDC_DATA[9] UART4_TXD/DATA[9] AUD3_RXD / COL CLK BT_USB_SRC[1]	10K-PD	LCD Data Bus
132	3V3	LD10	**LD10**	SLCDC_DATA[10] RTS_4 / DATA[10] AUD3_TXC / RX_ERR DAT0 / BT_MLC_SEL	10K-PD	LCD Data Bus
133	3V3	LD11	**LD11**	SLCDC_DATA[11] CTS_4 / DATA[11] AUD3_TXFS RDATA[2] / DAT1	10K-PD	LCD Data Bus
134	3V3	GPIO	A16	EIM_A[16] VEN1 / LCDC_REV	GPIO2[2]	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
135	3V3	GPIO	A14	EIM_DA_H2[14] CLK1 / LCDC_SPL	GPIO2[0]	Sampling start signal for left and right scanning.
136	3V3	LD12	**LD12**	SLCDC_DATA[12] MOSI / DATA[12] ROW[6] / RDATA[3] DAT2 / BT_SRC[0]		LCD Data Bus

PIN	Type	Function	i.MX25 Pad Name	Alternate functions	GPIO	Description (refer to I.MX25 manuals for details)
137	3V3	LD13	**LD13**	SLCDC_DATA[13] MISO / DATA[13] ROW[7] / TDATA[2] DAT3 / BT_SRC[1]		LCD Data Bus
138	3V3	LD14	**LD14**	SLCDC_DATA[14] SCLK / DATA[14] COL[6] / TDATA[3] AUD3_RXC BT_EEPROM_CFG	47K-PU	LCD Data Bus
139	3V3	LD15	**LD15**	SLCDC_DATA[15] RDY / DATA[15] COL[7] / RX_CLK AUD3_RXFS BT_UART_SRC[0]	10K-PD	LCD Data Bus
140	3V3	LD16 / GPIO	D15	EIM_D[15] / DAT7 **LCDC_LD[16]**	GPIO4[5]	LCD Data Bus
141	3V3	LD17 / GPIO	D14	EIM_D[14] / DAT6 **LCDC_LD[17]**	GPIO4[6]	LCD Data Bus
142	GND	GND				
143	3V3	HSYNC	**HSYNC**	SCL / BUFFER_EN VEN1 USBH2_DATA[4] BT_UART_SRC[1]	GPIO1[22] 10K-PD	Line Pulse or HSync
144	3V3	VSYNC	**VSYNC**	SDA / DMARQ / TX1 USBH2_DATA[5] BT_UART_SRC[2]	GPIO1[23] 10K-PD	Frame Sync or Vsync—This signal also serves as the clock signal output for gate; driver (dedicated signal SPS for Sharp panel HR-TFT)
145	3V3	OE_ACD	**OE_ACD**	SLCDC_RS SS0 / DA_1 / RX1 USBH2_DATA[7] BT_LPB_FREQ[1]	GPIO1[25] 47K-PU	Alternate Crystal Direction/Output Enable
146	3V3	LSCLK	**LSCLK**	SLCDC_CS DA_0 / PD1 USBH2_DATA[6] BT_LPB_FREQ[0]	GPIO1[24] 47K-PU	Shift Clock
147	GND	GND				
Module Specific Signals						
148	3V3	GPIO	A10		GPIO4[0]	
149	3V3	GPIO	A17	TX1 TX_ERR	GPIO2[3]	
150	3V3	GPIO	A18	PD1 COL	GPIO2[4]	
151	3V3	GPIO	A19	RX1 RX_ERR	GPIO2[5]	
152	3V3	GPIO	A20	CLK1 RDATA[2]	GPIO2[6]	
153	3V3	GPIO	A21	RST1 RDATA[3]	GPIO2[7]	
154	3V3	GPIO	A22	VEN1 TDATA[2]	GPIO2[8]	
155	3V3	GPIO	A23	TX1 TDATA[3]	GPIO2[9]	
156	3V3	GPIO	A24	PD1 RX_CLK	GPIO2[10]	
157	3V3	GPIO	A25	RX1 CRS	GPIO2[11]	
158	3V3	GPIO	CS0		GPIO4[2]	
159	3V3	GPIO	CS1	NANDF_CE3	GPIO4[3]	
160	GND	GND				
161	3V3	D[0]	D[0]			
162	3V3	D[1]	D[1]			
163	3V3	D[2]	D[2]			
164	3V3	D[3]	D[3]			
165	3V3	D[4]	D[4]			
166	3V3	D[5]	D[5]			
167	3V3	D[6]	D[6]			

PIN	Type	Function	i.MX25 Pad Name	Alternate functions	GPIO	Description (refer to I.MX25 manuals for details)
168	3V3	D[7]	D[7]			
169	3V3	A [0]	A [0]			
170	3V3	A [1]	A [1]			
171	GND	GND				
172	NVDD_DRYICE	TAMPER_A	TAMPER_A			DRYICE external tamper detect pins, active high. If either TAMPER_A or TAMPER_B asserted, then external tampering is detected. Should be tied to pull-down if no tamper detection is required on board.
173	NVDD_DRYICE	TAMPER_B	TAMPER_B			
174	NVDD_DRYICE	MESH_C	MESH_C			Wire-mesh tamper detect pins which can be routed at the PCB board to detect attempted tampering of a protected wire. MESH_C is active high and should be connected to an on-board pull-down if no tamper detection is required. MESH_D is active low and should be connected to an on-board pull-up if no tamper detection is required.
175	NVDD_DRYICE	MESH_D	MESH_D			
176	3V3	A [2]	A [2]			
177	3V3	A [3]	A [3]			
178	3V3	A [4]	A [4]			
179	3V3	A [5]	A [5]			
180	3V3	A [6]	A [6]			
181	3V3	A [7]	A [7]			
182	3V3	A [8]	A [8]			
183	GND	GND				
184	analog	REF	REF			Touchscreen ADC External reference voltage (2.5 V). REF may be left floating if the internally generated 2.5 V supply is enabled. Use of an external reference is recommended.
185	analog	XN	XN			Touscreen ADC input channels
186	analog	XP	XP			
187	analog	YN	YN			
188	analog	YP	YP			
189	analog	WIPER	WIPER			
190	analog	INAUX0	INAUX0			General purpose measurements channels
191	analog	INAUX1	INAUX1			
192	analog	INAUX2	INAUX2			
193	power	NVCC_DRYICE	NVCC_DRYICE			DRYICE power supply output. Source can be SoC supply or backup supply. This pin can be used to power external tamper detect components.
194	3V3	A [9]	A [9]			
195	3V3	A [11]	A [11]			
196	3V3	A [12]	A [12]			
197	NC					not connected
198	NC					not connected
199	NC					not connected
200	GND	GND	GND			